A Review on Multilevel Inverter Topology, Control Techniques and New E-Type Multilevel Inverter

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Abstract - The emergence of multilevel inverter has been increase since the last decade. The effort of the researchers and industry has led to a rapid development of different multilevel inverter topologies and modulation techniques. These new types of inverter are suitable for high voltage and high power application due to their ability to synthesis waveforms with better harmonic spectrum. Numerous topology have been introduced and widely studied for utility and drive application. In addition,a new E-type topology was introduced in this paper.`Each module produce 13 levels with four unequal dc source and 10 switches. Also this module is able to create negative level without any additional circuit. MATLAB simulation and practical results are presented to validate the e-type module good performance.

***Index Terms* – Asymmetric, components, E-Type multilevel inverter, H-Bridge, selective harmonic elimination**

I. INTRODUCTION

Power electronic inverters are widely used in industrial power conversion systems both for utility and drives applications (Tolbert and Peng 1998, 1999, 2002) [6]. As the power level increases, the voltage level also increases accordingly to obtain satisfactoryefficiency. The word "inverter" in the context of power electronics denotes aclass of powerconversion circuits that operates from a dc voltage source or a dc current source and converts it into ac voltage or current[11]-[12].Thus, for example, the primary source of input power may be utility ac voltage supply that is "converted", to dc by an ac to dcconverter and then "inverted" back to ac using an inverter. Here, the final output may be of a different frequency and magnitude than the input ac of the utility supply.Typical Applications such as Un-interruptiblePower Supply (UPS), Industrial (induction motor) drives, Traction, HVDC [4]-[5]. The different types of multilevel inerter available .A continuous development of multilevel inverter to drive the to drive the high voltage and high current industrial application [5]-[7].Nowadays multilevel inverter are good solution for power application due to the fact that they can achieve high power using advanced power semiconductor.

MULTI LEVEL INVERTERS (MLI)

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly [9]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not onlyachieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application .The concept of multilevel converters has been introduced since 1975[11]-[12].

Multilevel Inverters have been attracting attention in recent years due to high power quality, high voltage capability, low switching losses and low Electro Magnetic Interference (EMI) concerns; and have been proposed as the best choice in several medium and high voltage applications such as static VAR compensators and large electrical drives (Min 1999 and Peng 1996, 1997, 2001) [6]. Conventional inverter can switch to each input / output connection between two possible voltage (and possible current) levels. Multilevel inverter can switch their outputs between many voltage or current levels and have multiple voltage or current sources (or simply capacitors or inductors) as part of their structure. Although multilevel inverters were basically developed to reach higher voltage operation, before being restricted by semiconductor limitations, the extra switches and dc sources (supplied by dc-link capacitors) could be used to generate different voltage levels, enabling the generation of stepped waveform with less harmonic distortion, reducing dv/dt and common-mode voltages.in Static VAR compensation and in drive systems .

A proper starting value of modulation index and initial guess is necessary to solve these equations. Solving these transcendental equations with n number of unknowns is a tedious job. But the switching angles can be calculated offline to eliminate the specific low order harmonics and also switching takes place at the fundamental frequency and

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hence minimizes the switching losses (Jason et al 2007). In other words, only a few commutations take place in one cycle increasing efficiency and enabling air cooling. The computation of the switching angle increases with the increase in the voltage levels. With a limitation for the switching angles to be within (π/2), it provides a narrow range of modulation index. This method is limited to open-loop applications and low dynamic performance demanding applications (Cheng et al 2006) [9].which in turn leads to the increasing number of semiconductors and total standing voltage (TSV) of the module This paper aims to achieve maximum capacity from DC link by a suitable arrangement of switches which improves economic implementation cost, switching frequency, TSV, number of levels, and THD[13].

L.wang and d.zhand published power and voltage control of a three phase solid state transformer using micro grid application in 2016[3].S.Alishah published a new general multilevel converter topology based on cascaded connection of sub multilevel units with reduced component in 2016[5].F.Deng and Y.Tian published modular multilevel converter under sub module faults in 2016[15].R.Samanhakhsh published reduction of power electronic components in multilevel converter using new switched capacitor diode in 2016[10].E.Samadaei published asymmetric multilevel inverter with reduced components in2016[3].And finally overcome this paper new hybrid topology of e-type cascaded with H-Bridge with reduced count.

One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in themultilevel converter and, therefore, the active semiconductor cost is not appreciably increased when compared with the two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power convertersthat the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing [2].To some extent, the voltage balancing can be addressed by using redundant switching states, which exist due to the high number of semiconductor devices. However, for a complete solution to the voltage-balancing problem, another multilevel converter may be required [3].

II. MULTILEVEL INVERTER TOPOLOGIES

This chapter gives the brief description of conventional inverters with their advantages and disadvantages. Topologies of various multilevel inverters such as diode clamped, flying capacitor and cascaded H-bridge with their concepts are discussed.

The main drawback of multilevel inverters is that the number of switches increases with the number of levels. In early stages of multilevel inverters, development of control circuitry for large number of power switches was a significant problem. But continuous evolution of CPLD, DSP and FPGA devices easily solved this inconvenience. Other drawback of this inverter is the requirement ofmultiple numbers of DC voltage sources, mainly provided by capacitors. Balancing the voltage sources during operation under different load conditions is an important challenge.

In spite of these drawbacks, introducing multilevel inverters will decrease switching losses occurred in the power device. By comparing with two level inverters, smaller size filter is required for the elimination of harmonics. This reduces the inverter weight, dimension and cost. Many multilevel inverter topologies have been proposed during the last two decades. Contemporary research has evolved novel inverter topologies and unique modulation schemes. Moreover, three different major multilevel inverter structures have been reported in the literature. They are,

- Diode clamped /Neutral clamped Multilevel Inverter
- Flying capacitors /Capacitor clamped Multilevel inverter
- CascadedH-bridge Multilevel Inverter

MULTILEVEL CONCEPT

The concept of multilevel inverters has been introduced since 1975. However, the elementary concept of a multilevel inverter to achieve high power is to use a series of power semiconductor switches with several low voltage DC sources to perform power conversion by synthesizing a staircase voltage waveform. One phase leg of multilevel inverter is shown in Figure1. In this schematic diagram, operations of semiconductors are shown by an ideal switch with several states.

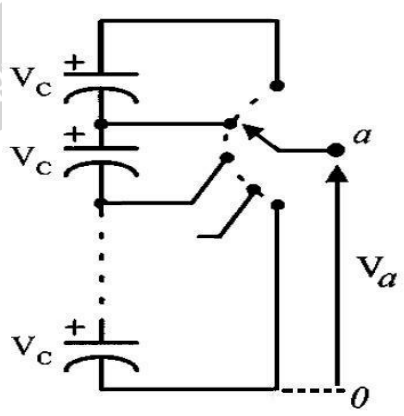

Fig 1: One phase leg of a multilevel inverter

Nearly for the three decades, multilevel inverters are being used in the world of power electronics. They are named by the number of voltage levels they generate and the different topologies they have. Usually the number of output voltage levels is odd instead of even. It means that the definition of a zero voltage level in the output of inverter, like in three

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level or in five level inverters, makes it more sinusoidal with less harmonics.

Diode Clamped Multilevel Inverter

One of the traditionally accepted and widely used topology for various industrial and power sector applications is neutral point converter which was proposed by Nabae, Takahashi and Akagi in 1981.The diode-clamped multilevel inverter employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. However, as the number of levels has increased the number of clamping diodes, switching devices and dc capacitors also increases, thus the circuit configuration becomes more complicated.

Ingeneral, for an *m*-level diode clamped inverter, for each leg *2(m-1)* switching devices, *(m-1) * (m-2)* clamping diodes and *(m-1)* dclink capacitors are required. This topology also suffers the disadvantage of unequal load distribution among the semiconductor switches particularly, when the inverter runs under pulse width modulation (PWM) technique, the reverse recovery of the clamping diodes is also a major design challenge. Though, the operation of NPC topology is simple and straightforward but as the number of inverter levels increases, number of devices increases. Hence, design and implementation becomes so complicated for higher number of levels.

Flying Capacitor Multilevel Inverter

The Flying capacitor alternatively known as capacitor clamped inverter topology which was proposed by Meynard and Foch in 1992.This inverter topology is similar to that of the NPC topology except the usage of clamping diodes. This topology inverter uses capacitors instead of clamping diodes. Flying capacitor MLI has capacitors on dc side and connected like ladder structure, where the voltage across each capacitor differs from that of the next capacitor.

One important advantage of the flying-capacitor topology is that it has phase redundancies for inner voltage levels; in other words, two or more valid switch combinations are possible to synthesize an output voltage whereas diode clamped inverter has only line-line redundancies.Generally for an m-level output phase voltage will requires, *(m-1) * (m-2)/2* auxiliary capacitors per phase in addition to *(m-1)* maindc link capacitors under the assumption that the voltage rating of the capacitors is identical to that of the main switches.

Cascaded H-Bridge Multilevel Inverter

The concept of series H-bridge inverter was first proposed by R. H.Baker and L. H. Banister in 1975 [38]. In order to overcome thedrawbacks ofNPC and FC topologies such as extra clamping diodes and capacitors, Marchesoni.M.,et.al have proposed Cascaded H-Bridge Inverter.The basic idea of connecting single-phase H-Bridgeinverters in cascade with multiple isolated dc supplies to realize multilevel waveforms was first introduced in 1990 for plasma stabilization.

Each Separate DC Source (SDCS) is connected to a single phase full bridge or H-bridge inverter (Anup Kumar Panda & Yellasiri Suresh 2012). A single phase structure of eleven level cascaded inverter is illustrated.The number of output phase voltage levels (N_L) in a cascaded inverter is defined by $N_L = 2s+1$, where s is the number of separate DC sources. Output phase voltage V_{an} is given in Equation.

Van = va1 + va2 + va3 + va4 + va5

III. MODULATION TECHNIQUES

Modulation is the process of switching the power electronic device in a power converter from one state to another. All modulations are aimed at generating a stepped waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency and phase fundamental component that is usually sinusoidal in steady state. Each topology has different switching configuration to achieve commanded output voltage. Modulation strategies are responsible for synthesizing reference control signals and for keeping all voltage sources balanced.

Space Vector Modulation

Each multilevel inverter has several switching states which generate different voltage vectors and can be used to modulate the reference (Govindaraju & Baskaran 2010). In SVM, the reference signal is generated from its closest signals. Some vectors have redundant switching states, meaning that they can be generated by more than one switching state. This feature is used to balance the capacitor voltages (Govindaraju & Baskaran 2010, Amit Kumar Gupta & Ashwin Khambadkone 2007). Multilevel SVM must manage this behavior to optimize the search for the modulating vectors and apply an appropriateswitching sequence (Wenxi Yao et al 2008). A conceptually different control method for multilevel converters, based on the space-vector theory, has been introduced, which is called space vector control.

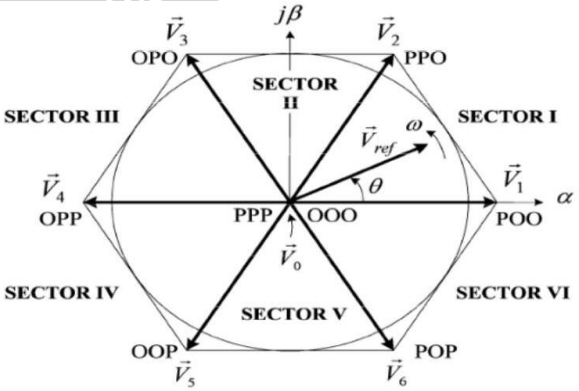

Fig 2. Space Vector Modulation

Selective Harmonic Elimination

Selective harmonic elimination technique is one of the traditionally preferred modulation techniques in control of multilevel inverter since early 1960s. SHE technique was first introduced by Patel H.S., et al, to eliminate some

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selected harmonics in half-bridge and full-bridge inverter output waveforms. SHE can also be called as preprogrammed pulse width optimum modulation technique which provides a superior harmonic profile with minimum switching frequency or switching losses.In spite of these advantages, SHE has drawbacks of heavy computational burden in solving nonlinear transcendental trigonometric equations and complicated hardware implementation.

These advantages have made SHE technique as a preferred modulation technique compared to other techniques in applications such as high-power medium voltage drives, high voltage direct current transmission, power quality improvement techniques, distribution generation systems and dual frequency induction heating.

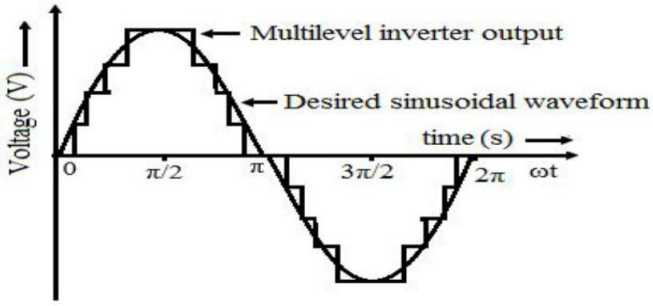


Fig 3. Stepped voltage waveform of multilevel inverter

Sinusoidal pulse width modulation

Sinusoidal PWM method is also known as the triangulation, sub harmonic, sub oscillation method, Carrier Based Pulse Width Modulation (CB-PWM) is very popular in industrial applications (Mohamed Dahidah & Vassilios Agelidis 2008).For realizing SPWM, a high frequency triangular carrier wave is compared with a sinusoidal reference of the desired frequency. The intersection of sinusoidal reference and triangular waves determines the switching instantsand commutation of the modulated pulse. Operating with constant frequency of carrier signal concentrates on voltage harmonics around switching frequency (which is of double the carrier frequency) and multiples of switching frequency. Carrier based modulation for more than two level inverters require more carrier signals. For N_L -level inverter, minimum (N_L -1) carrier signals are needed.Based on traditional sinusoidal pulse width modulation with triangular carriers, several multilevel carrier based pulse width modulation techniques have been proposed to reduce %THD in output voltage.

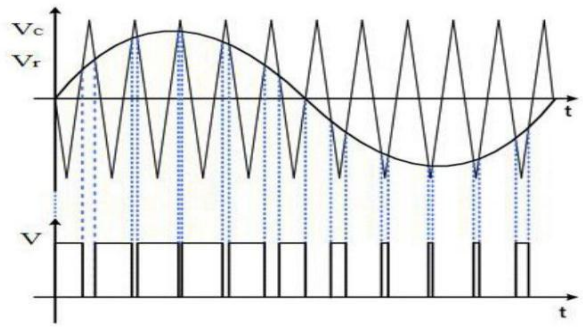


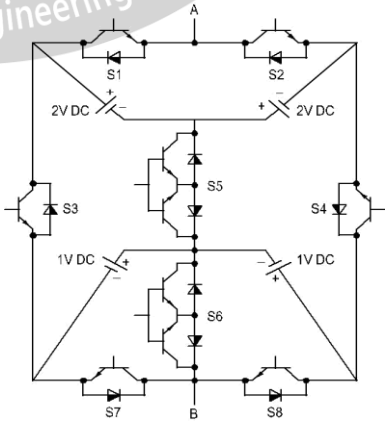
Fig 4. Sinusoidal pulse width modulation

Carrier Disposition Method

These techniques are usually applied to the neutral point clamped topology. These techniques may not be used for the H-Bridge inverter applications directly. But by using discontinuous PWM reference signals with phase-shifted carrier strategy may be implemented to apply PD technique to the H bridge inverter. Also these modulation techniques can be applied to asymmetric multilevel inverter, diode clamped MLI, flying capacitor MLI and other hybrid MLI configurations.

IV. E-TYPE MLI

This project introduces a new topology of asymmetric multilevel modular with a new component arrangement including10switches,10 diodes and 4 unequal DC sources (two2,two1V) named as Envelope type(E-Type). This arrangement synthesizes voltage sources produces 13 levels (positive level, 6 negative level and zero level) without any additional circuit. The main concept of this circuit is to create different paths from different sides of a DC source to be connected to other sources. Fig.3 shows the configuration of E-Type asymmetrical module in where DC sources are located in the middle of the circuit and are connected togetherto form different voltage levels via surrounding switch (S1-S6). A bidirectional switch (S7) is required to avoid short circuit of DC sources on left or right sides of the module. Another bidirectionalswitch(S8) isalsoneededto achievevoltage levels of $\pm 5V$



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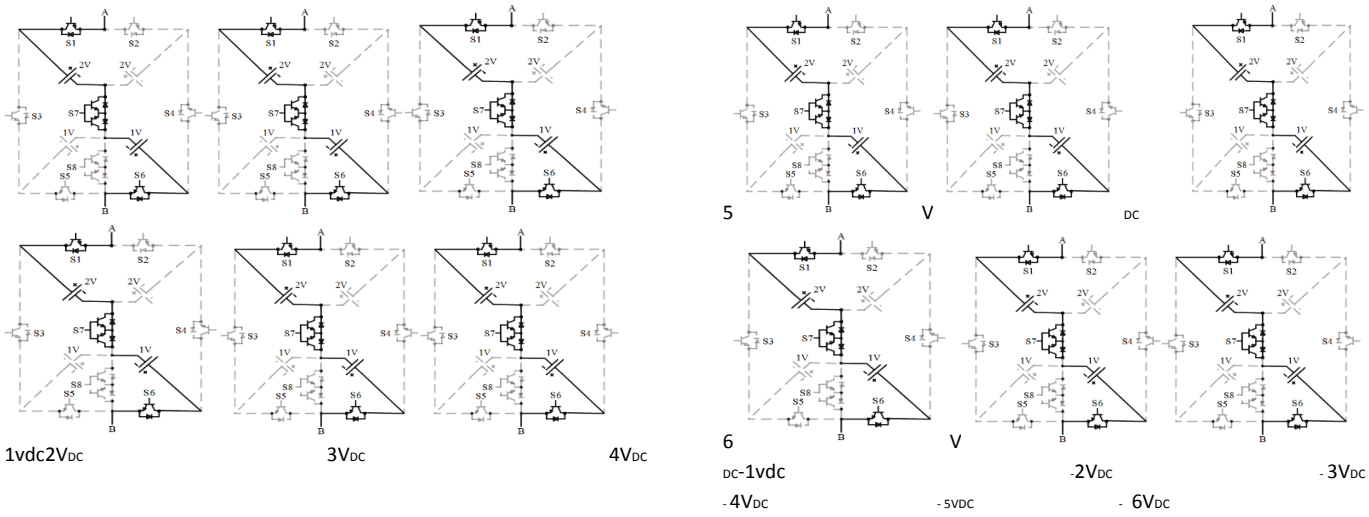

Fig 5. Existing E-Type module inverter circuit topology and different switch status

Table I Switching Table

		S1	S2	S3	S4	S5	S6	S7	S8
POSITIVE LEVEL	1VDC	1	0	0	0	0	1	1	0
	2VDC	1	0	0	0	0	0	1	1
	3VDC	1	0	0	0	1	0	1	0
	4VDC	1	0	0	1	0	1	0	0
	5VDC	1	0	0	1	0	0	0	1
	6VDC	1	0	0	1	1	0	0	0
NEGATIVE LEVEL	-1VDC	0	1	0	0	1	0	1	0
	-2VDC	0	1	0	0	0	0	1	1
	-3VDC	0	1	0	0	0	1	1	0
	-4VDC	0	1	1	0	1	0	0	0
	-5VDC	0	1	1	0	0	0	0	1
	-6VDC	0	1	1	0	0	1	0	0

As shown in Table I, switch pairs(S_1, S4) levels, respectively. In addition, (S_1, S_2) and (S_3,S_4) cannot be on at the same time.Fig.4shows output voltage of the proposed inverter with the associated pulse pattern in one cycle of fundamental voltage. As shown inFig.4, switches S_1,S_2,S_3,S_4 and S_7 a returned on and off in low frequency, which reduces switching losses to a great extent. Other switches also operate in a reasonable switching frequency. Table II shows numberof voltage levels, semiconductor components, DC sources and drivers based on number of module units (n) and number of desired levels (N_L).

Table II Equation of e-type module

	BASED ON NUMBER OF MODULE UNITS	BASED ON NUMBER OF DESIRED LEVELS
Levels	13n+1	N_L
Number of switches	10n	$5(N_L-1)/6$
Number of diodes	10n	$5(N_L-1)/6$
Driver	8n	$8(N_L-1)/6$
Number of DC Links	4n	$4(N_L-1)/6$
TSV	20n	$10(N_L-1)/6$

V .RESULT AND DISCUSSION

Experimental results are carried out to verify the results of simulation and analysis in order to achieve a 13- level sinusoidal waveform with THD% 6.35%. Each levelis considered 5 volts. The fundamental output voltage and totalharmonic distortioncalculated by using FFT analysis window. The input voltage of e-type module is 21 v and peak voltage (output voltage) is 30 v. Figure 6 shows output voltage and current waveform of simulated module and figure 7 shows THD waveform.

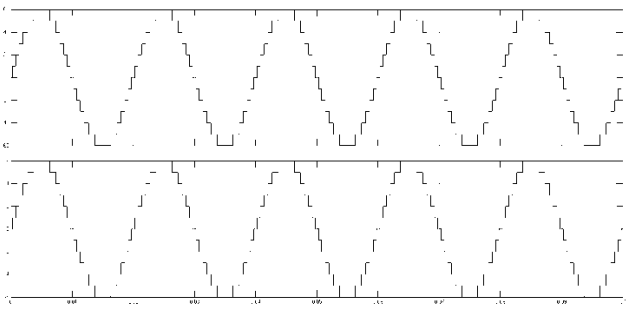

Fig 6. Output voltage and current waveform

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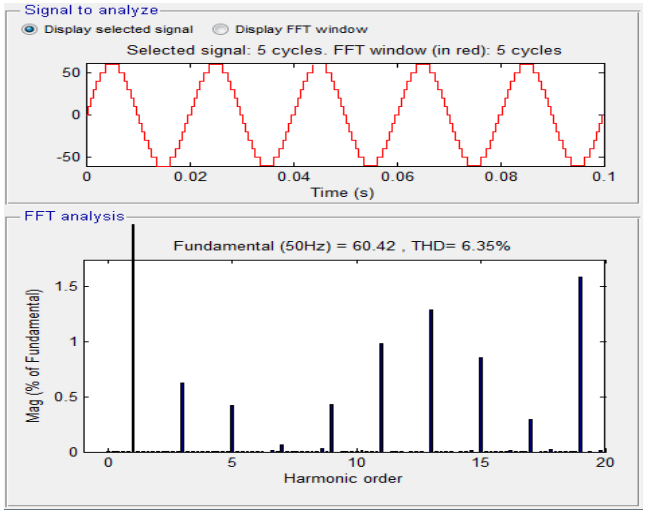

Fig 7. Output voltage and THD using FFT analysis

VI. CONCLUSION

This paper presented several topologies for multilevel inverters (MLI), some of them well known with applications on the market. Every topology have been described in detail. Several modulation techniques have also been presented which are to be used with the presented topologies andthis paper presented a new multilevel inverter topology named as Envelope Type (E-Type) module which can generate 13 levels with reduced components. It can be used in high voltage high power applications with unequal DC sources. As hybrid module can be easily modularized, it can be used in cascade arrangements to form high voltage outputs with low stress on semiconductors and lowering the number of devices. Modular connection of these modules leads to achieve more voltage levels with different possible paths. It causes an improvement in the reliability of the modular inverter which enables it to use different paths in case of malfunction for a switch or a driver.THD v% is obtained 6.35% in simulation and experimental results, respectively that satisfy harmonics standard (IEEE519).

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