International Journal for Research in Engineering Application & Management (IJREAM)
ISSN : 2454-9150 Vol-04, Issue-03, June 2018

CMOS Design Analysis of 4 Bit Shifters

[1]Baljot Kaur, M.E Scholar, Department of Electronics & Communication Engineering, National Institute of Technical Teachers Training & Research, Chandigarh, UT, (India), jotbabbar94@gmail.com

[2] Rajesh Mehra, Associate Professor, Department of Electronics & Communication Engineering, National Institute of Technical Teachers Training & Research, Chandigarh, UT, (India)

Abstract - This paper presents CMOS shifters which are designed to reduce area as well as power on 90nm technology. Two designs for shifters have been proposed namely fully automatic and semi-custom. In first approach fully automatic design where inbuilt active devices are used along with auto-routing and placement options. In second approach, semi-custom design inbuilt active devices are used along with optimized manual routing and placement. In fully-automatic approach proposed schematic is designed with DSCH and its equivalent layout is created using Microwind. In case of semi-custom design, optimized layout is created with Microwind. It can be observed from simulated results that SIPO area is reduced by 48.55% and power is reduced by 7.30% whereas in PIPO area is reduced by 52.71% and power is reduced by 2.5%. It is well known that as computation point of view PIPO is used. As Circuit is mimicked and the power and area consumption is less in PIPO so we can use it in many applications.

Keywords: flip flop, semiconductor, shift register-P-MOS,N-MOS, Transistor.

I. INTRODUCTION

Shift Registers in digital circuits are used to shift as well as store the data. That's why there need is increasing day by day. Shifters are used in manipulation of data as well as multiplication of floating numbers etc. The fast development in semiconductor gadget industry has prompted the improvement of high versatile frameworks with upgraded unwavering quality [1]. Those convenient applications, become critical to limit area [2] and utilization because of the restricted accessibility of battery control [1]. That's why, area minimization, power dissipation turns into a vital plan in VLSI [3,4]. In shift registers flip flops are cascaded, having a similar clock, in which the output of one flip-flop is connected with the input of the other flip-flop in the chain, bringing about a circuit that moves one bit in every clock pulse, moving in the information show at its information and moving out the last piece in the array. Shift Register is of two types Parallel and Serial inputs types and Parallel and Serial outputs types. Depending on this further four types of shift registers are there Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out, Parallel In Parallel Out. In this Shift register we can either use J-K flip flop or D flip flop whereas in this paper D flip flop is used to reduce the complexity. Repeating waveforms can be generated for counter circuits by using shift registers. Shift Registers which has complex circuitry will take long time to generate feedback patterns so they can resemble random noise or pseudo noise. Some of the methods are suggested in this paper to implement that type of shift registers[5]. As ,given above there are four types of shift registers given below as [6]:

1. SISO (Serial In Serial Out):Data is shifted serially in one by one bit and shifted serially out one by one bit. It takes n bits to shift data in and n-1 bits to shift data out.
2. SIPO (serial In Serial Out):Data is shifted serially in one by one bit and shifted parallel out. It takes n bits to shift data in and 0 bits to shift data out.
3. PISO (Parallel In Serial Out):Data is shifted parallel in and shifted serially out one by one bit. It takes 1 bit to shift data in and n-1 bits to shift data out.
4. PIPO (Parallel In Parallel Out):Data is shifted parallel in and parallel out. It takes 1 bit to shift data in and 0 bit to shift data out.

II. SHIFTERS

Serial In and Parallel Out shift register is the type of shift register in which data will load and retrieve in serial and parallel mode respectively. Below Figure 1 is shown how SIPO is working.

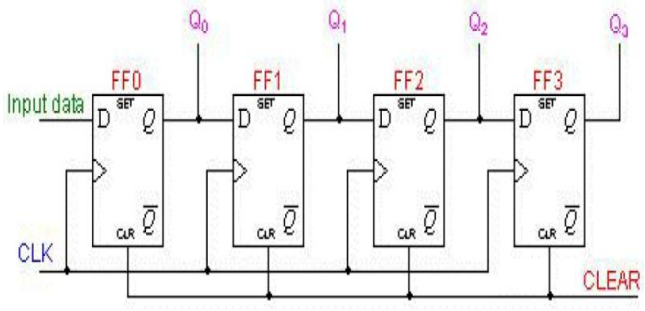

Figure 1: Serial In Parallel Out Shift Register

 DOI : 10.18231/2454-9150.2018.0367

Its working is simple as data entered serially one by one bit. Output is taken parallel all the bits simultaneously. To enter data serially n clock pulses are required. To take data parallel out 0 clock pulses are required[7]. Operation of SIPO is as initially, we apply reset or clear so that any previous data stored in the shifter can be removed. When clear is given to the circuit all the flip flops are at low state i.e. zero. When flip flops are at low state output of the circuit will be zero. When first clock signal appeared, then data transfer takes place. In first flip flop which is suppose QA will receive the first bit of data it becomes 1 and other flip flops become low i.e. zero. When second clock signal appeared, in second flip flop which is suppose QB will receive the second bit of data it becomes 1 and other flip flops become low i.e. zero. When third clock signal appeared, in third flip flop which is suppose QC will receive the third bit of data it becomes 1 and other flip flops become low i.e. zero. When last clock signal appeared, in fourth flip flop which is suppose QD will receive the fourth bit of data it becomes 1 and other flip flops become low i.e. zero. At every clock pulse, it will shift the data . Output of one flip flop become the input of other[8].

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

Figure 2: Truth Table of SIPO

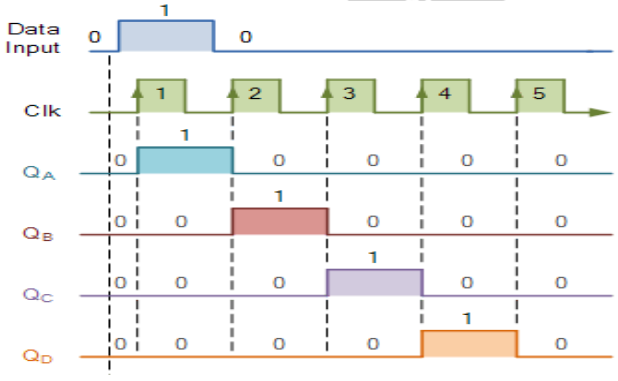

Figure 3: Waveform of SIPO

The above shown truth table of SIPO explains that when no clock signal is provided , no output is achieved. When clock is applied QA becomes high and other remains low i.e. 0. At the second clock pulse, QB will become high and other remains low. When third clock pulse arrives, QC becomes high and other remains low. A last clock pulse QD becomes high and other becomes low.

Parallel In and Parallel Out shift register is the type of shift register in which data will load and retrieve in parallel mode. Below Figure 4 is shown how PIPO is working.

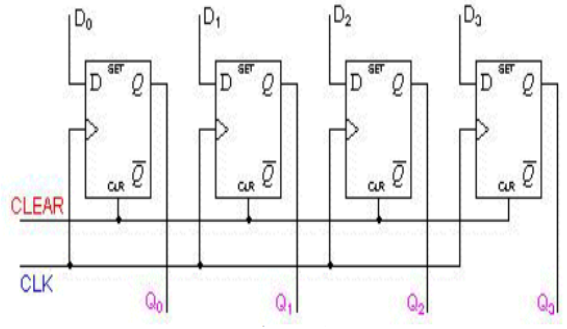

Figure 4: Parallel In Parallel Out Shift Register.

Its working is extremely straightforward when contrasted with other shift registers. As shown in the Figure 1 all flip flops are connected with CLEAR. CLEAR is used to clear or reset the flip flop so that if there is any previous data stored in it will be removed and it can be used for future purposes. First Step is to CLEAR all the flip flops and output from Q_0 to Q_3 are at logic'0'. Next step is to provide CLOCK to every flip flop. When logic '1' given to the CLOCK then shift register starts working. Input D_0 is given to the first D flip flop and output is taken from the Q_0. Likewise all the four flip flops are connected and inputs are given corresponding to all the four flip flops. D_1 input is given to the second flip flop and output is taken from the Q_1. D_2 input is given to the third flip flop and output will be taken from Q_2. D_3 input is given to the last flip flop and output will be taken from Q_3. Let us take an example for better understanding . Suppose we have data 0100 i. e D_0 '0', D_1'1', D_2'0', D_3'0' then after one clock pulse output will be Q_0 '0', Q_1'1', Q_2'0', Q_3'0' [9]. This is shown that we need only one clock pulse to enter the given data and output in 0 clock pulse because it work in parallel mode it will give the output as soon as input is received.

As shown in Truth Table Initially shift register was RESET. When CLOCK signal is provided then only shifting of data takes place. In first clock pulse 1 is shifted from first flip flop to second. In second clock pulse that one is shifted to the third flip flop and first flop will get new data[10]. Likewise process keeps on going and at last all the flip flops will get some data i. e '1111'. The clock is used to shift data one place to the right side.

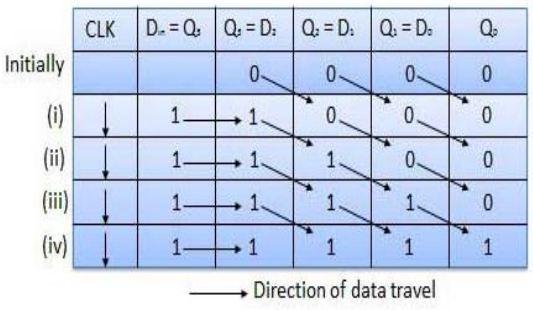

Figure 5: Truth-Table of Shift Register.

 DOI : 10.18231/2454-9150.2018.0367

III. SIMULATION & RESULTS

In DSCH software it deals with graphical or circuit diagram where focus is to draw circuit diagram and apply inputs and outputs respectively. As shown below the circuit diagram of SIPO having clock and clear along with inputs and outputs. From DSCH verilog file is generated.

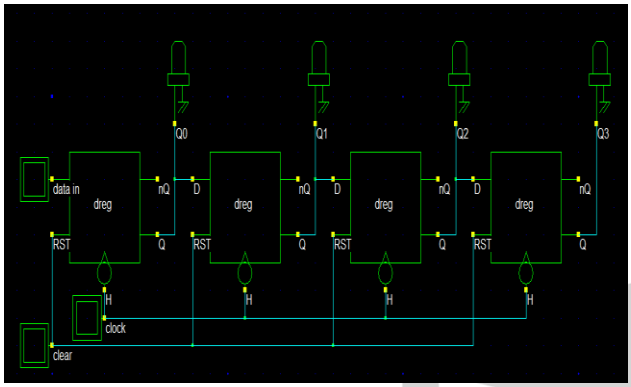

Figure 6: DSCH design of SIPO

Working of SIPO in DSCH software is shown in below Figure 7. When clock signal is given and corresponding inputs are given then their corresponding LEDs will glow.

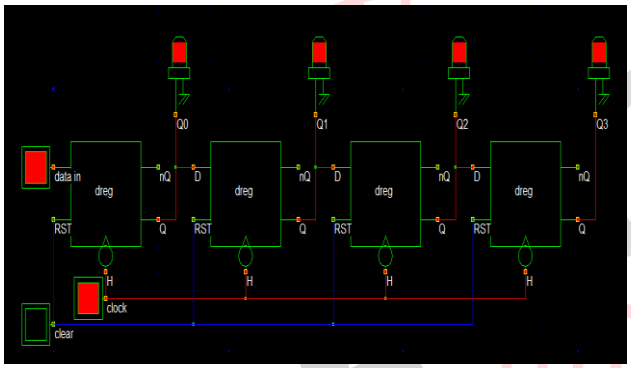

Figure 7: DSCH design of working SIPO

Waveform generated in DSCH during its operation is shown in Figure 8. Serial data is given and parallel output is achieved by the circuit which is shown below.

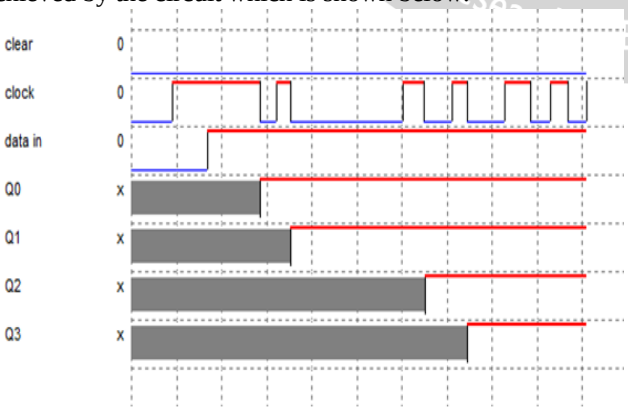

Figure 8: Waveform of SIPO

Below shown in figure 9 is the result in Microwind software which is taken after compiling in Microwind. It gives the Layout structure.

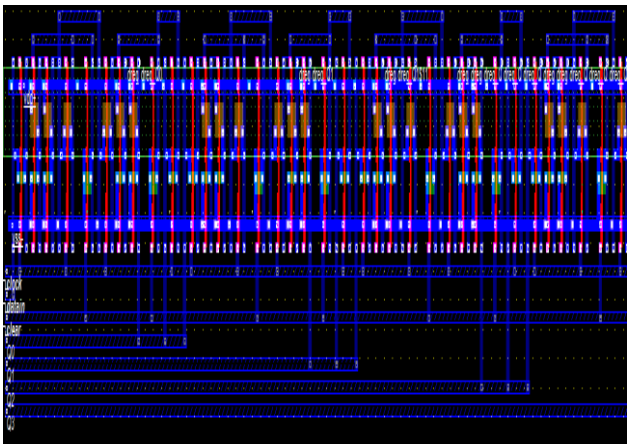

Figure 9: Fully-automatic SIPO

Below shown are simulation result of layout structure in Microwind. In this waveforms are shown with respect to different inputs respective outputs are shown.

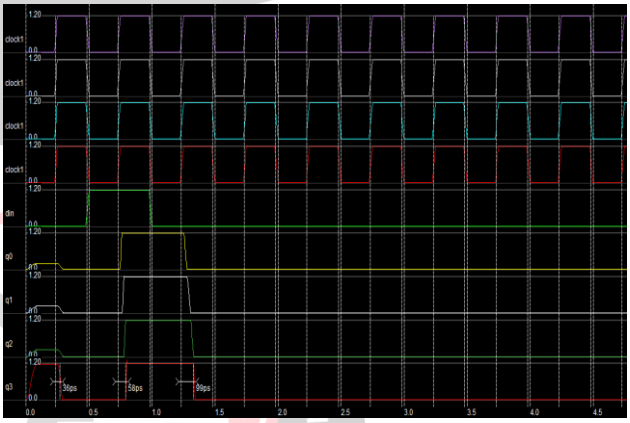

Figure 10: Voltage vs Time graph

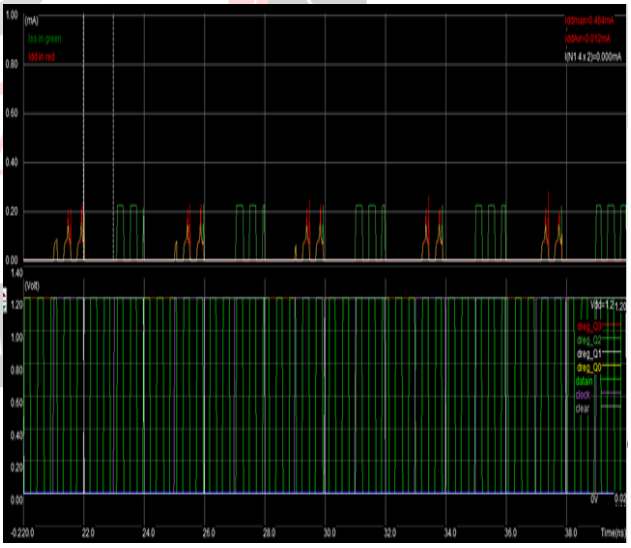

Figure 11: Voltage vs Current graph

In DSCH software it deals with graphical or circuit diagram where focus is to draw circuit diagram and apply inputs and outputs respectively. As shown below the circuit diagram of PIPO having clock and clear along with inputs and outputs. From DSCH verilog file is generated.

 DOI : 10.18231/2454-9150.2018.0367

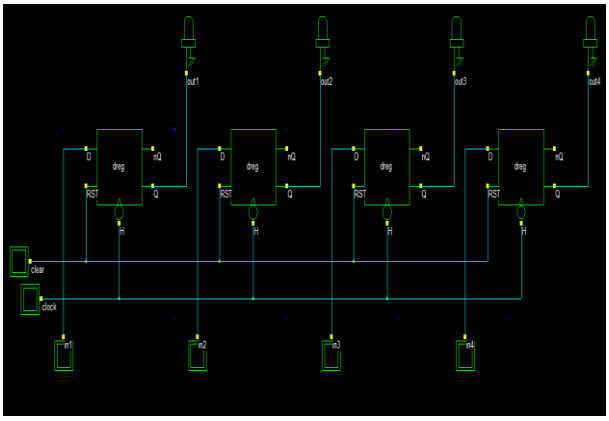

Figure 11: DSCH design of PIPO

Working of PIPO in DSCH software is shown in below Figure 7. When clock signal is given and corresponding inputs are given then their corresponding LEDs will glow

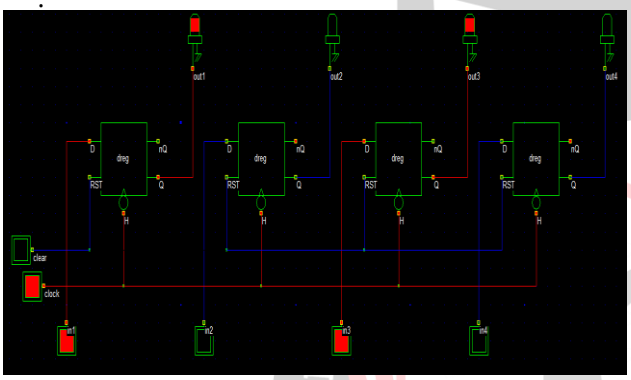

Figure 12: DSCH design of working PIPO

Waveform generated in DSCH during its operation is shown in Figure 8. Parallel data is given and parallel output is achieved by the circuit which is shown below.

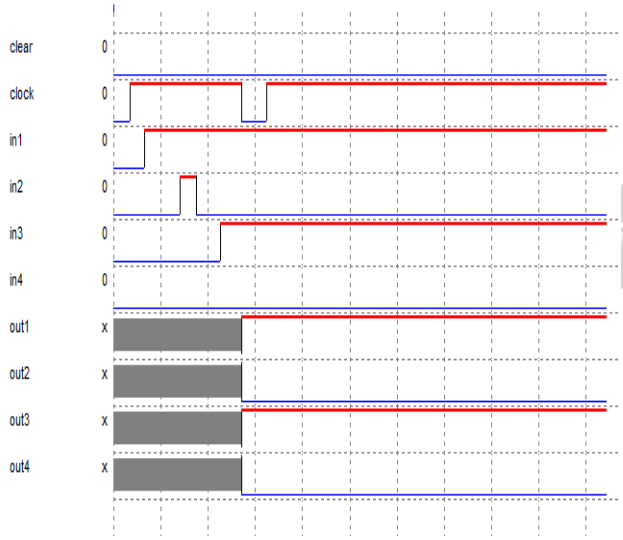

Figure 13: Waveform of PIPO

Below shown in figure 14 is the result in Microwind software which is taken after compiling in Microwind. It gives the Layout structure.

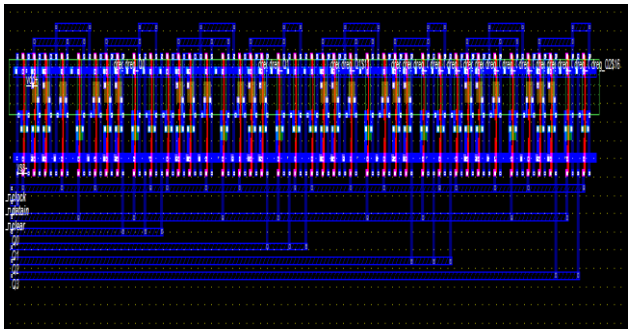

Figure 14: Fully-automatic PIPO

Below shown are simulation result of layout structure in Microwind. In this waveforms are shown with respect to different inputs respective outputs are shown.

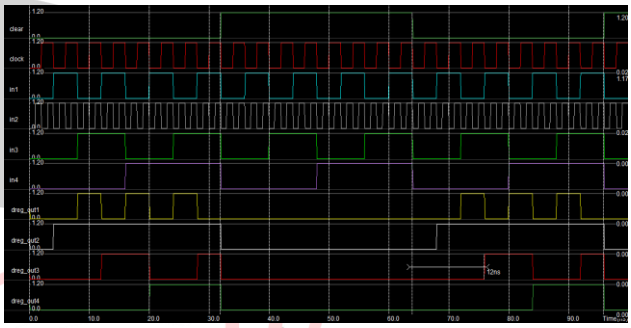

Figure 15: Voltage vs Time graph

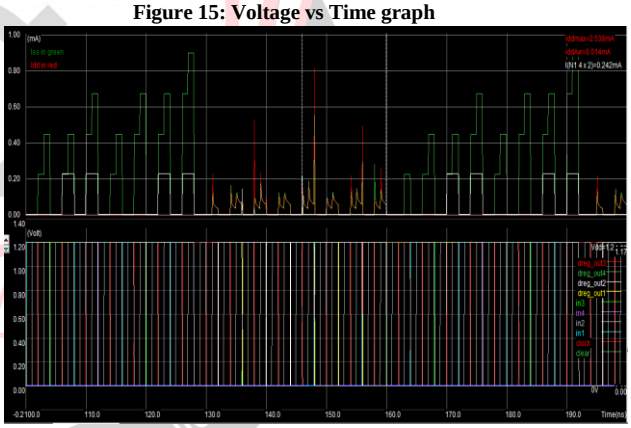

Figure 16: Voltage Vs Current graph

Figure 17 shows semi-custom design of SIPO shifter where different D flip-flops are used to complete the circuit. D flip-flops are built using NAND gates. Overall area of this layout is reduced.

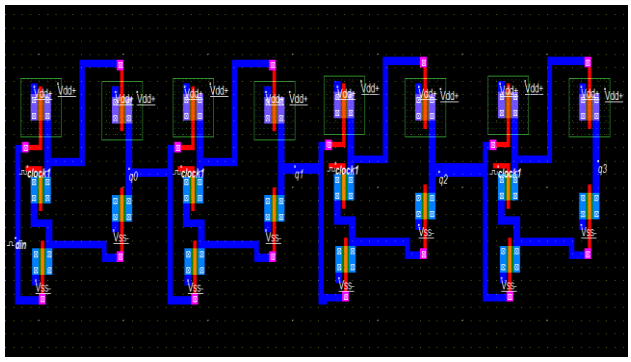

Figure 17:Semi-custom SIPO.

 DOI : 10.18231/2454-9150.2018.0367

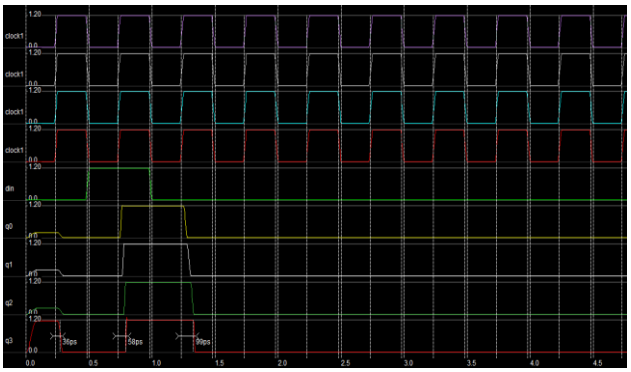

Figure 18: Voltage vs Time graph

Figure 18,19 shows the simulation result of semi-custom layout design of SIPO shifter. Different waveforms are shown with respect to different inputs their respective outputs are shown.

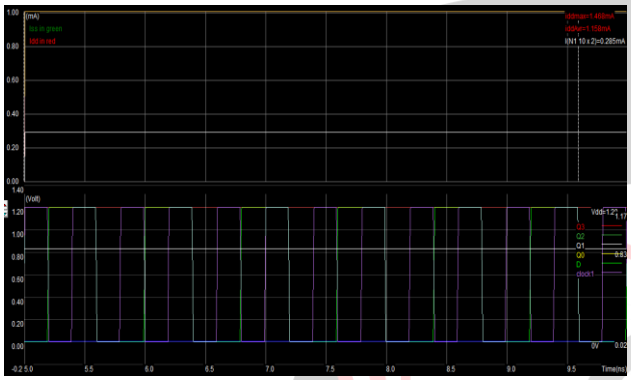

Figure 19: Voltage Vs Current graph

Figure 20 shows semi-custom design of PIPO shifter where different D flip-flops are used to complete the circuit. D flip-flops are built using NAND gates. Overall area of this layout is reduced.

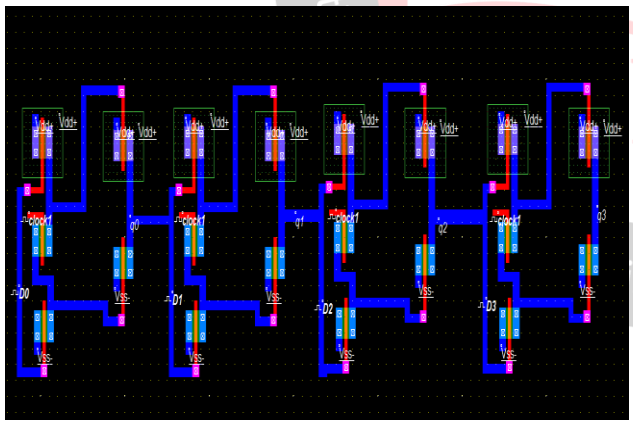

Figure. 20: Semi-custom PIPO.

Figure 21,22 shows the simulation result of semi-custom layout design of SIPO shifter. Different waveforms are shown with respect to different inputs their respective outputs are shown.

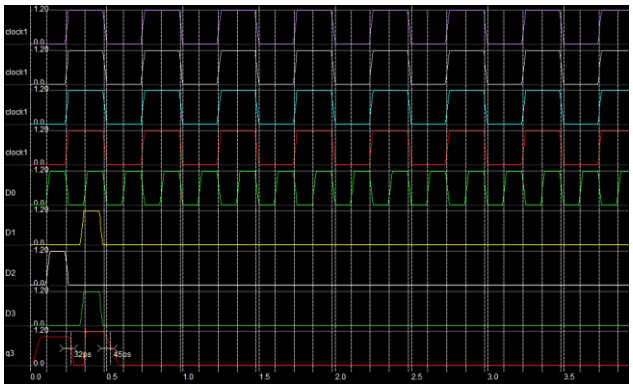

Figure 21: Voltage vs Time graph

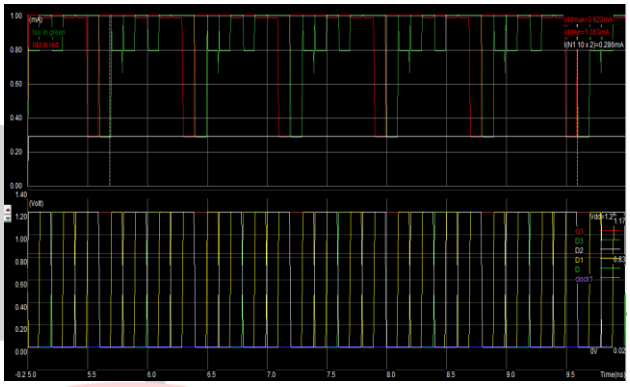

Figure 22: Voltage vs Current graph

Table 1: Area and Power consideration.

Serial In Parallel Out			
Method	Technology(nm)	Area (μm^2)	Power (µW)
Fully-automatic	90	228.4	9.85
Semi-custom	90	117.5	9.136
Parallel In Parallel Out			
Method	Technology(nm)	Area (μm^2)	Power (µW)
Fully-automatic	90	248.5	6.211
Semi-custom	90	117.5	6.052

The parameters under consideration are area and power. Table 1 shows area and power consumption of 4 bit Serial In Parallel Out and Parallel In Parallel Out shift register.

V.CONCLUSION

The analysis of two different shifters with same technologies is done in this paper. As shown Fully-automatic and Semi-custom layout design are generated for 4 bit SIPO and PIPO to analyze area and power consumption. In semi-custom method, SIPO area is reduced by 110.9 μm^2 whereas in PIPO area is reduced by 131 μm^2. In semi-custom method, SIPO power is reduced by 0.69 µW whereas in PIPO power is reduced by 0.159 µW. It is well known that as computation point of view PIPO is used. Because it consumes less power as compared to SIPO. From the above simulation it can be analyze that semi custom design is more efficient in terms of area and power. Where area minimization is essential in those applications semi-custom design can be implemented.

 DOI : 10.18231/2454-9150.2018.0367

VI. ACKNOWLEDGEMENT

The authors would like to thank the Director, National Institute of Technical Teachers' Training & Research, Chandigarh, India for continuous support throughout this research work.

REFRENCES

[1] Borivoje Nikolic, "Design in the Power–Limited Scaling Regime", IEEE Transactions on Electron Devices, Vol.55, No. 1, pp.71-83, 2008.

[2] International Technology : Roadmap for Semiconductors:www.itrs.net/Links/2005ITRS/Design 2005 .pdf.

[3] N. A. Whitaker, Jr, M. C. Gabriel, H.Avramopoulos, and A. Huang"All-optical, all-fiber circulating shift register with an inverter", Optics Letters, Vol. 16, Issue 24, pp. 1999-2001,1991

[4] Davida, G.I. and Rodrigues, "Data Compression Using Linear Feedback Shift Registers", Proceedings of the IEEE Data Compression Conference, Los Alamitos, 1994

[5] Moon, T. K. and Veeramachaneni. S. "Linear Feedback Shift Registers as Vector Quantisation Codebooks", Electronics Letters, Vol. 35, No. 22, pp. 1919-1920,1999

[6] Deepak subramanyan, B.S. and Adrian Nunez, "Analysis of Sub-threshold Leakage Reduction in CMOS Digital Circuits", Proceedings of the 13th NASA VLSI Symposium, USA, June 5-6,2007

[7] Wayne Wolf, "Modern VLSI Design (System on chip Design)", Pearson Education, pp. 319-321.

[8] Akhilesh Verma, Rajesh Mehra, "Design and Analysis of Conventional and Ratioed Cmos Logic Circuit" IOSR Journal of VLSI and Signal Processing Vol.2, pp. 25-29, April 2013

[9] Harmeet Singh "Efficient Layout Design of CMOS Full Subtractor" Int. Journal of Electrical & Electronics Engg. Vol. 2, Spl. Issue 1 (2015).

[10] Monikashree T.S,Usharani.S, Dr.J.S.Baligar "Design and Implementation of Full Subtractor using CMOS 180nm Technology" International Journal of Science, Engineering and Technology Research (IJSETR), pp 1421-1426, Vol. 3, Issue 5, May 2014.

 DOI : 10.18231/2454-9150.2018.0367