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Design Of QC LDPC Code Encoder Using Dual Diagonal Matrix

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Abstract: - **An efficient encoder for IEEE802.16e LDPC code is proposed in this paper. This design utilizes the common dual-diagonal structure in parity matrix to avoid the inverse matrix operation which requires extensive computations. Parallel, matrix vector multiplication (MVM) units, bidirectional operation and storage compression techniques are applied to this encoder to increase the encoding speed and significantly reduce the logic elements.**

Synthesis report shows that this LDPC encoder design uses lesser area with increased encoding speed.

I. INTRODUCTION

Low-Density Parity-Check was originally proposed by Robert Gallager in 1962. It was proposed as a class of channel coding. For implementing these codes a large amount of computing power is needed due to high complexity and requirements of memory for encoding/decoding operations, so they were forgotten, After few years turbo codes were introduced. David MaCkAY showed and proved that Ldpc codes were also capable of approaching The Shannon limit using iterative decoding techniques.

An Ldpc code is a linear block code. It is recognized by a very sparse parity-check matrix. This means that the parity check matrix has a very low concentration of 1's in it That's why it is known as Low-Density Parity-Check code. The sparseness of Ldpc code is the characteristic which can lead to excellent performance in terms of bit error rates.

Ldpc codes are the most preferred types of codes for practical applications in comuunication and storage system. It provides detectiion or correction of the errors which occur in a communication through a noisy quantum channel. Ldpc codes are knwon as practical class of classical error correcting codes due to its compact representation and good performance, especially for short code lengths. Its characterization is easily testable for not only theoretical use but also for computer experiments.

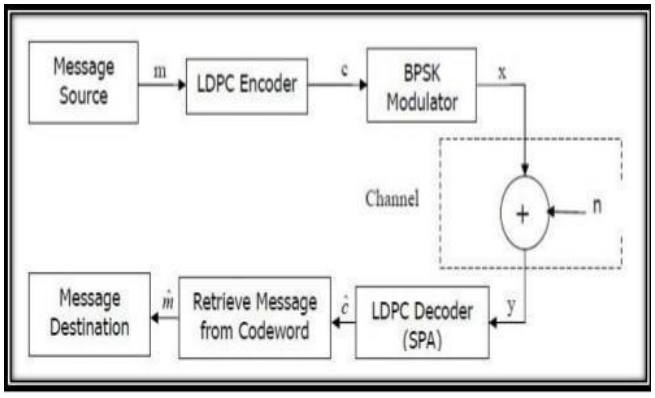
It provides high performance error-correction scheme. Ldpc codes are promising candidates for next generation wireless communication standards.

This code can be obtained by a discrete mathematical characterization for module.

Gallager publishes the existence of the class of Ldpc codes in 1960. But he didn't provided the idea how to generate the parity-check matrix. It is also known as the 'H' matrix. There are many methods proposed by various researchers for generation of parity-check matrix. Those methods include:-

- Random Generation subject to constraints
- Density Evolution
- Finite Geometry

There are various keys to examine parity-check matrix when generating it. It includes minimum distance, cycle length and linear independence.



II. LITRATURE REVIEW

Sridhar et al (2001), analyzes LDPC codes based on permutation matrices which accommodate a variety of code rates and code lengths was constructed. In their work, a block structured parity check matrix of size j. k was constructed. Each element of this matrix was permuted square matrices. An (155, 64) LDPC code with minimum distance of 20 was constructed from permuted identity matrices with row and column weights of 5 and 3 respectively. The results show that the performance of these

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codes compared well with that of randomly constructed codes for block lengths less than 10,000 bits.

Mansour & Shanbhag(2002) They both together reduced the complexity of the parallel decoder architecture, they eliminated the need of the complex interconnection network and the algorithm performance promised was retained by random codes' BCJR algorithm is used to compute reliability metrics. It reduces the message switching activity in the decoder compared to the approaches existing at that time The results of the simulation showed that the approach proposed by the authors had a power savings of up to 85.64% over conventional implementations.

Chen & Hocevar (2003) In this paper the ASIC and FPGA implementation of rate ^{X}A, 8088bits irregular LDPC decoder was presented The decoder achieved a throughput of 40 Mbps and 188 Mbps using FPGA and ASIC. To reduce the overall decoding latency and power consumption the early stopping circuit was used.

Wang & Cui (2007) A memory efficient partially parallel decoder architecture suited for high rate quasi cyclic LDPC codes was proposed. They used modified min sum algorithm for decoding he check to variable messages were stored in a compressed form where only minimum, sub minimum, index of minimum and signs of all the messages corresponding to one row were stored as one entry. A data distributor was used to extract individual messages from the compressed form. The proposed design achieved 30% memory reduction over traditional architectures.

Liu & Shi (2008) He introduced a new Sliced Message Passing (SMP) decoding algorithm in which the total number of variable to check messages were sliced into equal chunks and computation then performed chunk by chunk. This new scheme broke the tie between the check and variable node stages and achieved increased throughput. The SMP decoder for a 2048 bit (6,32) implemented in an IBM CMOS 90-nm process achieved a higher throughput and hardware utilization efficiency.

Mohsenin & Baas (2010) In this paper he proposed a Split decoding algorithm in which row processing was partitioned into two blocks. Here, the row processing in each partition was performed using only the input messages contained within its own partition. A significant error performance loss resulted

Xiang et al (2011) He presented a partially parallel Dual path fully overlapped QC-LDPC decoder for WiMax system. He introduced a symmetrical six stage pipelining to improve the throughput. The memory access conflicts were eliminated by block row and column interleaving, base matrix reordering and partitioning of the memory. The decoder was configurable to support different code parameters of WiMax system The LDPC decoder fabricated in the SMIC 0.13um CMOS process attained a throughput of 847-955 Mbps and it occupied an area of 4.84mm^2.

III. BACKGROUND

A. QC-LDPC Codes in IEEE 802.11ac Standard

The parity check matrix of QC-LDPC codes can be described as a base parity check matrix. Fig. 1 shows an Example of the base parity check matrix defined in IEEE 802.1 lac standards [2]. The digit of the base parity check

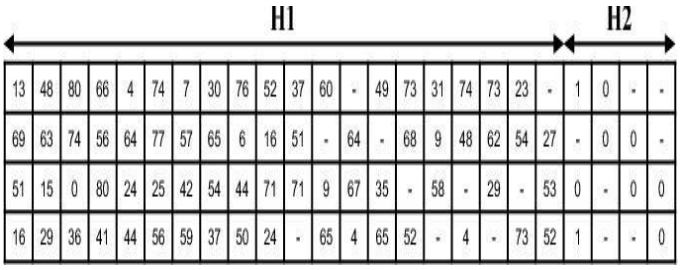

Fig 2 Base Parity check matrix of QC-LDPC codes

Code rates	1/2,2/3,3/4,5/6
Codeword block lengths	648,1296,1944
Sub-matrix sizes Z	27,54,81

Fig 3 QC-LDPC code parameters

Matrix indicates the right cyclic shift values of the identity Z x Z square sub-MATRIX. The dash '-' indicates the zero one. Fig 3 shows the QC-LDPC codes parameters of IEEE 802.1 lac standards. The QC-LDPC encoder has to support 4 code rates, i.e., 1/2, 2/3, 3/4 and 5/6, and 3codeword block lengths, i.e., 648, 1296 and 1944. To Support 3 codeword block lengths, sub-matrix sizes Z are defined as 27, 54 and 81. In IEEE 802.1 lac standards, 12 base parity check matrices are defined to support 4 code rates and 3 codeword block lengths

B. Linear Encoding Process

The base parity check matrix can be partitioned into the two sub-matrices as shown in Fig. 1. Let H = [HI H2] be the partitioned base parity check matrix, where HI is an (N-M) x M sub-matrix, and H2 is an (N-M) x (N-M) Matrix. Let c = [m p] be a codeword block, where m and P indicate the information bit sequence and the parity bit Sequence, respectively. From the property that the correct Codeword satisfies the parity check equation, the parity bit sequence p can be derived as follows,

$$H.C^T = H_{1.m}{}^T + H_{2.P}{}^T = 0, \qquad (1)$$

$$P^{T=}H_2{}^{-1}.H_{1.m}{}^T \qquad (2)$$

IV. METHODOLOGY

First of all, it is very important to understand the ldpc codes and what is dual diagonal matrix.

Quasi-cyclic low density parity-check (QC-LDPC) codes are defined by a sparse matrix. It has received much attention as a forward error correction code because they have excellent error correction performance. QC-Ldpc encoder provides high throughput and a compatible rate. Small number of clock cycles has to be performed in encoding process to achieve high throughput. The LDPC

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encoders can support various code rates and codeword block lengths.

The LDPC encoder can provide 3.34 Gbps throughput. For efficient QC-LDPC encoder, it consider four types of rotate-left-accumulator circuits. The formation of QC-LDPC code's parity check matrix is by ZxZ square sub-matrices. Each sub-matrix is an identity matrix with a cyclic shift or zero matrix. Information bit sequence is multiplied by the parity check matrix during an encoding process.In parity check matrix, ZxZ square sub matrix is multiplied to the one Zxl sub sequence of the information bits. The multiplication can be implemented by a cyclic shifter due to the cyclic shift property of the sub-matrix. Many cyclic shifters are required to achieve high throughput. This is the reason, the design of cyclic shifter is an important issue in QC-LDPC encoder.

In this paper, we propose a high throughput QC-LDPC encoder by adopting the dual-diagonal matrix. Based on dual-diagonal matrix, we propose high throughput QC-LDPC encoder design. The goal of the encoder design is to use less number of logic elements. The proposed encoder is also rate compatible to support various code rates and codeword block lengths.

A. Encoding of Ldpc encoder

It is mainly comprises of two tasks:
1.Construct a sparse parity-check matrix.
2.Generate codeword using this matrix.

Encoding Scheme	Description	Comments
Generator matrix Product	H=G ;c=Ug[l]	Use Sparse generator matrices Bad error floor.
Triangular System Solving	Using Back substitution as much as possible	High complexity post processing.
Iterative encoding	Solve Hc[l]=0 using the sum product algorithm	Such iterative encodable codes have weak performance.
Cyclic encoding	Multiplications with a shift register	Few constructions

In encoding process, construction of parity check matrix is very important. They play vital role in the design of LDPC encoder. We have used dual-diagonal parity check matrix for the LDPC Encoder.The main advantage of using dual diagonal matrix is that it reduces the complexity in the process of computation. It can solve the complex codes easily.

B. QC-LDPC codes with a dual diagonal parity-structure

QC-LDPC codes having long codes can be encoded with low complexity. Using shift registers, the encoder of QC-LDPC codes can be implemented. In this implementation encoding would be linearly proportional to the code length. The parity-check matrix H can be partitioned into square sub-blocks of size ZxZ in QC-LDPC code. In it we take three sub-block sizes as Z=27, Z=54,Z=81.

Then i,j be ZxZ zero sub-block or identity matrix I with permutation which is located at i-th row and j-th column with k times. Cyclic shift is 0<k<Z to the right.
Parity check matrix H with basic sub-blocks matrices P, .mZxnZ is defined as

$$H = \begin{bmatrix} P_{0,0} & P_{0,1} & P_{0,2} & \cdots & P_{0,n_b-2} & P_{0,n_b-1} \\ P_{1,0} & P_{1,1} & P_{1,2} & \cdots & P_{1,n_b-2} & P_{1,n_b-1} \\ P_{2,0} & P_{2,1} & P_{2,2} & \cdots & P_{2,n_b-2} & P_{2,n_b-1} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\ P_{m_b-1,0} & P_{m_b-1,1} & P_{m_b-1,2} & \cdots & P_{m_b-1,n_b-2} & P_{m_b-1,n_b-1} \end{bmatrix}$$

The QC-LDPC codes are symmetric which are latest and gives high throughput. It encodes an size k,s=(sO,sl,...,sk-information block which is ofl)^T of size into a codeword vector c n,c=(sO,sl,...,sk-l,pO,pl,...pn-k-l)^T, by adding n-k parity bits obtained so that it must satisfy the equation given below,

H . c = 0

Where

H = parity-check matrix.

Then the matrix H is divided into two region. **Hs** is the sub-matrix for region where systematic bits are multiplied and **Hp** represents the region where parity portion of codeword is multiplied to H matrix such that

H = [Hs Hp]

The parity of portion of matrix Hp can be further decomposed into two sub matrices as

Where

0 = identity matrix IZxZwith zero cyclic shift. Vectorlike sub-matrix hpis composed of weight-3 columns

hO = the cyclic shift at 1st row.

Consequently, matrix Hp becomes a dual-diagonal structure.

C. Encoding procedures for QC-LDPC codes

Due to high value for codeword length(n), LDPC coding poses computational overhead and hence the complexity increases in the process of encoding a LDPC encoder. LDPC computational overhead is proportional to m o r m . As n increases, the overhead increases significantly. Richardson discovered the method to overcome this issue. The amount of computation required in encoding was reduced by this method. Dual-diagonal parity structure has greatly reduced the encoding complexity so that computational overhead is proportion to n.

We will compare our proposed encoding scheme to Richardson's scheme

D. Conventional efficient encoding scheme

Richardson, et al proposed the efficient encoding scheme in which H is assumed as approximate lower triangular form. The parity-check matrix H is in the form,

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$$H = \begin{bmatrix} A & B & T \\ C & D & E \end{bmatrix}$$

Where ,
A =Z(m-l)xZ(n-m)
B=Z(m-l)xZ
T=(m-Z)x(m-Z)
C=ZxZ(n-m)
D=ZxZ
E=ZxZ(m-1)

The sub-matrices A and C corresponds to symmetric part Hs and under Hp sub-matrices B, D, T, E comes. Then vector hp becomes,

$$hp=[B^T D^T]^T$$

T is lower triangular with identity matrices along the diagonal and all the sub-matrices are sparse.

The matrix H is summarized with vector c then we get the equation,

$$A_s + Bpo + Tp1 = 0$$

$$(-ET^{-1}A + C)s + (-ET^{-1}B + D)_{po} = 0$$

Where,

$-ET'' = Z$ x Z sub-block.

It is obtained by sub-block addition operation (i.e. **I -I +I - I..... -I +I**) which accumulates columns of sub-matrix **A.** Note that,

$$-ET - 1B + D = I$$

Since addition of all sub-block matrices at weight-3 part of matrix **H**p suggested in standards such as [1] result simply ZxZ identity matrix **I.** Sloving Equation leads to direct solution of parity vectors **p**0 and **p**1 Thus, each parity bit vectors can be induced as,

$$p0 = (-ET^{-1}A + C)s$$

$$Tp^1 = As + B0,$$

p0 is obtained through accumulation of input bits. For p0 to obtain p1, block accumulation done exploiting dual-diagonal lower triangular matrix **T**.

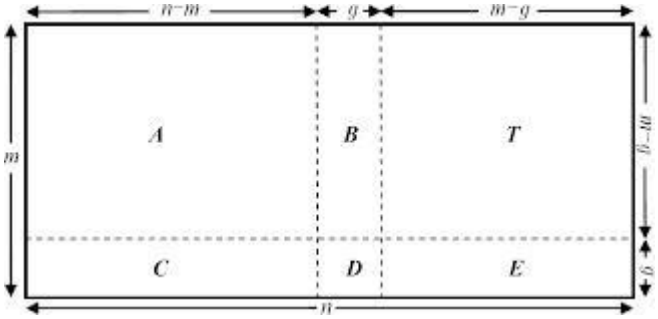

Fig.5 the parity-check matrix H and its sub-matrix size

IV. PROPOSED ENCODING SCHEME

In the proposed design of Encoder we have reduced the number of logic elements. An encoder has various code rate. It may be 1/2,2/3,3/4,5/6. As we know code rate and code word is an important part of encoding. Figure shown below is the block diagram of LDPC encoder.

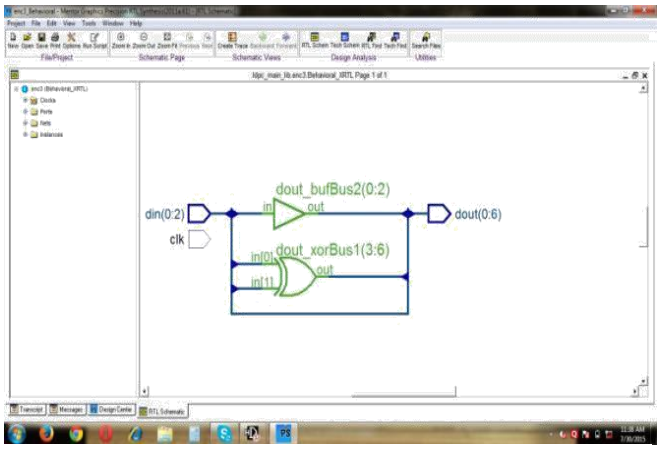

Fig 6 Diagram of Encoder

In our proposed LDPC encoder we have prefer the code rate 5/6. It is preferred to acquire less area. Proposed encoder can use less area. Number of logic elements used in the proposed encoder is less than the conventional encoder. The proposed encoder acquires less complexity as generation and calculation of the parity matrix is going on simultaneously. As both generation and calculation is going simultaneously, it saves time of computation. The proposed encoder is also rate compatible rather in conventional encoder first shifting is done for generating the parity matrix then after parity calculation was done and it acquires a lot of computation time and increases the complexity.

It consists of only two matrixes in which one is diagonal matrix and other is cyclic shift which further divided in sub matrices. Sub-blocks are of 16x16. That's why it consists 24 matrices vertically and 120 matrixes horizontally. The calculation done in the proposed encoder is block-wise so that we can use less registers and le number of logic elements. For the calculation of circular shift matrix we use rotator in the proposed encoder. So that computation complexity will be less. Input data used in the proposed QC-LDPC encoder is 120x16 bits. Input data(K) taken for the proposed encoder is 1920 bits. Encoder (N) is of 2304 bits. Therefore we get the parity bits of 384 bits

Parity bits (M) = Encoder (N)-Input data (K)

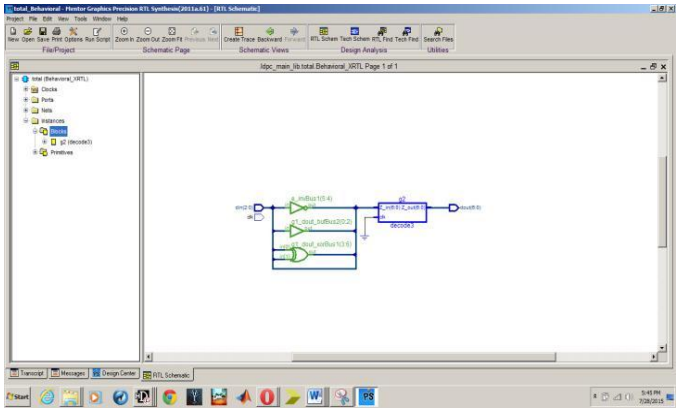

Fig 7 Schematic diagram of the encoder

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Figure shown above is the schematic diagram of the encoder. The codes are applied to generate the QC-LDPC codes. The number of LUTs used is 7 and time delay is 1.46ns. Cyclic shifter is used to reduce the complexity of the computation. Results prove that the proposed QC-LDPC Encoder is using less number of logic elements and reduces the complexity of the computations.

V. RESULT AND ANALYSIS

The proposed QC-LDPC encoder uses less number of logic elements and reduces the complexity of the computation. Computation was done block wise and this shows the result in reducing the number of logic elements. In this proposed encoder generating of parity bits and calculations are done simultaneously. This also saves time of computation as both process are going on simultaneously. The figure shown below shows the summary of the devices used in the designing of the QC-LDPC codes. Cyclic shifter is used to reduce the complexity of the computation.

Results prove that the proposed QC-LDPC Encoder is using less number of logic elements and reduces the complexity of the computations. The codes are applied to generate the QC-LDPC codes. The number of LUTs used in 7 and time delay is 1.46ns.

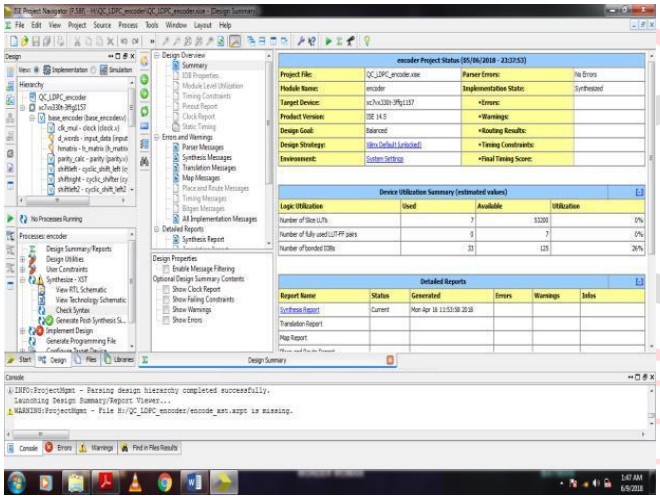

Fig 8 Summary of device used

Parameters	BASE	PROPOSED
No. of logic elements	11399	3363
No. of RAM used	According to the code rate used	2

Fig 9 Comparision between Base and Proposed

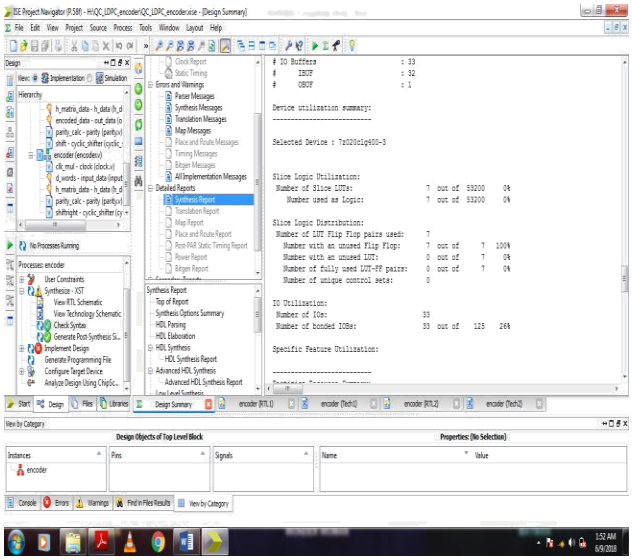

Fig 10 Representing the utilization of the device

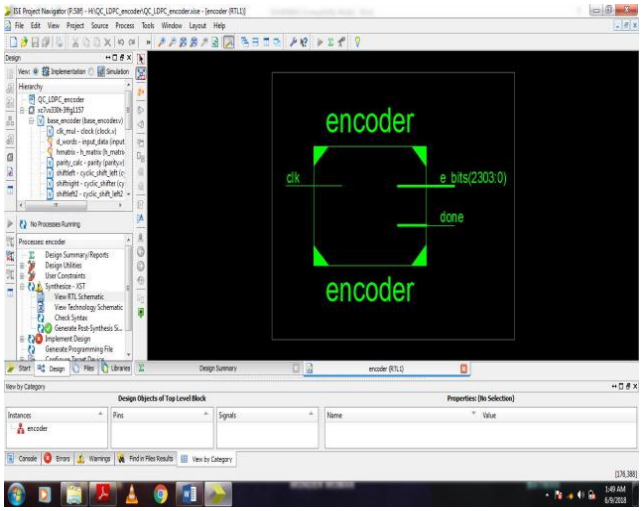

Fig 11. RTL schematic design of encoder

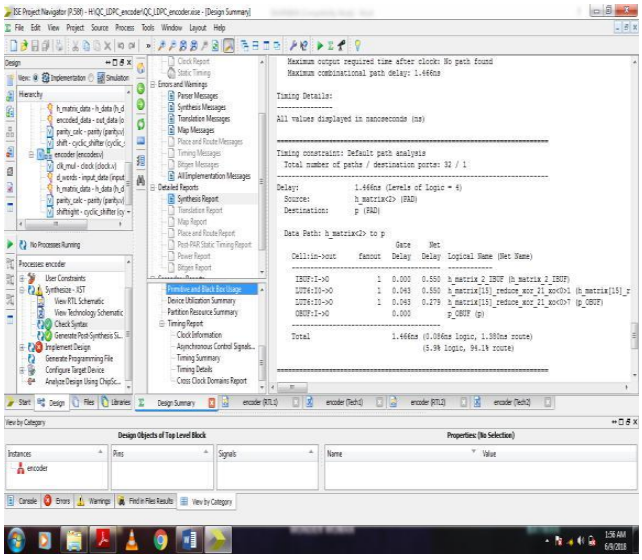

Fig 12. Estimated delay report

VI. CONCLUSION

In this paper, we proposed an QC LDPC encoder which uses less number of logic elements. By using the dual-diagonal matrix in the proposed encoder we have reduced

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the complexity of the system. As the generation and the computation of the parity check matrix is going on simultaneously in the proposed encoder rather than first generate the parity check matrix and then compute it. It saves time. Uses of cyclic shifter and rotator helps in computation and the proposed QC LDPC encoder uses less number of logic elements. The delay time of the proposed encoder is 1.46 ns.

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BIOGRAPHY

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