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Dynamic Power Analysis of CMOS Inverter with Various Parameters

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Abstract - In order to reduce power dissipation, many new techniques have been proposed and adopted for VLSI design. Modifications at the architecture to minimize the number of building blocks, optimizing the sub-systems to minimize the switching activity and circuit level design techniques to minimize power at the transistor level are the major techniques that are adopted. Multipliers and adders are the major building blocks of signal and 4G communication systems. In order to reduce power dissipation it is required to understand the sources of power consumption and it helps in understanding the schemes for low power design.

Key words: VLSI design, optimizing the sub-systems, switching activity, minimize power, Multipliers and adders.

I. INTRODUTION

1.1 SOURCES OF POWER CONSUMPTION IN VLSI

To measure the power consumption in any CMOS circuits the sources of power consumption should be known. Figure1 represents the sources of power consumed in a CMOS. The major part of the power consumption is Active and Standby power.

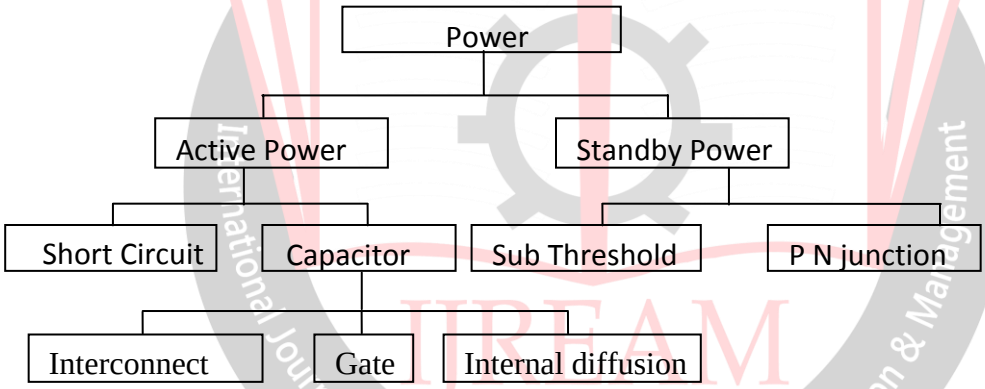

Figure1 Sources of power consumption in CMOS circuits

The active power consists of two components: (i) Capacitive or Dynamic power

(ii) Short Circuit power

Capacitive power is due to capacitive loads. Capacitive loads include interconnects, output gate capacitance and input gate capacitance.

The standby mode consists of two components: (i) Sub threshold

The junction power is due to PN junctions in a MOS device. In this work, assuming junction power as negligible only three components of power dissipation is considered to be for a given circuit as shown in Figure2.

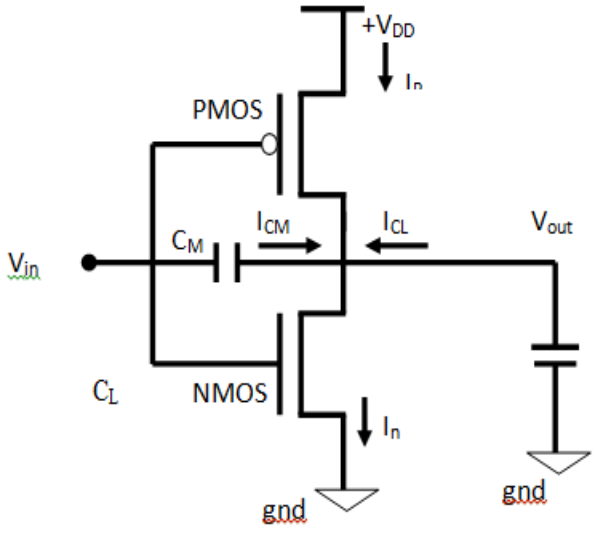

Figure 2 Power consumption components of a CMOS Inverter

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The gate capacitance C_M is an internal capacitance, connected between the common point of the gate of NMOS and PMOS with drain of NMOS. The Load capacitance C_L is made up of bulk to drain capacitances of both PMOS and NMOS, interconnect capacitance and gate capacitance of the load. During transition of input and output of an inverter, charging current (I_p), discharging current (I_n), I_{CM} and I_{CL} are of prime importance for power analysis as they are used to charge and discharge the load capacitance. These currents are the sources of power dissipation, as they get diffused into the ground during circuit transition [1].

Capacitive or Dynamic Switching Power

During the output voltage logic transition period (charging and discharging of the load capacitance), the power dissipated at that period is called as dynamic power. When the input changes from 0(Low) to 1(High), PMOS device changes its state from ON to OFF. During this state, PMOS transistor changes from linear to cutoff region as shown in Figure3. The charging current from V_{DD} charges the load capacitance during input being logic '1'. When input switches from logic '1' to '0', NMOS goes from cutoff region to saturation and PMOS remains in cutoff condition. The load capacitance C_L discharges through NMOS to ground as shown in Figure 4. For lossless power the charging current is equal to discharging current, else, the difference turns into power loss.

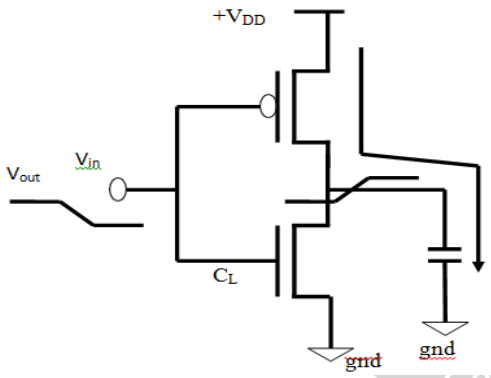


Figure3 Dynamic power of CMOS Inverter

The average power dissipation of the logic gate, driven by periodic input with ideally zero input rise and input fall-times, can be calculated from the charge up and charge down of total output load capacitance C_L as given in Equation 1.

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} Vout\left(-Cload * \frac{dVout}{dt}\right)dt + \int_{T/2}^{T}(Vdd - Vout)\left(Cload * \frac{dVout}{dt}\right)dt\right]$$

By evaluating this integral, the expression for the average dynamic power consumption in CMOS logic circuits leads to Equation 2

$$P_{avg} = \alpha_t * V_{dd}^2 * Cload * f_{clk} \quad \ldots(2)$$

α_t represents the node transition factor, which is the effective number of power-consuming voltage transitions per cycle.

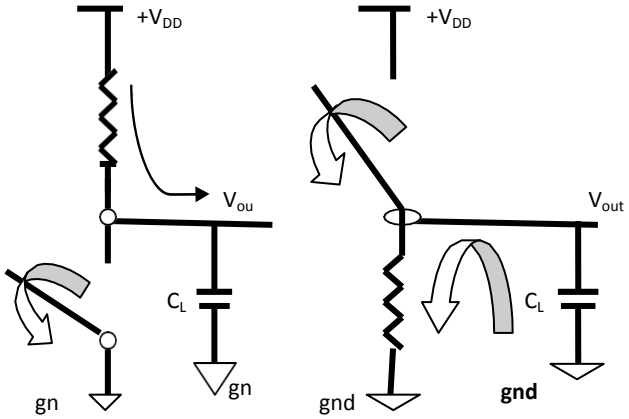
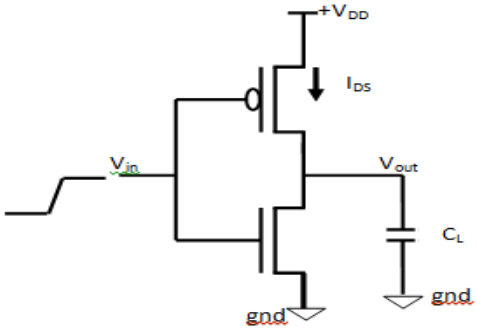


Figure 4 Charging and Discharging of load capacitance C_L

Short-Circuit Power

During input switching, there would be a point at which both NMOS and the PMOS transistors are conducting simultaneously and the power supply is directly connected to ground for a short interval of time as shown in Figure 5. This current is limited by transistor's current capacity that depends on transistor size. Figure 6 shows the short circuit current that occurs in CMOS capacitor with small load capacitance C_L due to input switching. It appears only for a short interval during transition.

Figure 5 CMOS transistor with I_{sc} during switching



$t_{sc} = (V_{dd} - 2V_t) * t_r / (V_{dd} * 0.8)$ ..... $(3P_{sc} = t_{sc} * I_{peak} * V_{dd} * f$ ..... (4)

Where I_{peak} - Peak current of transistor at $V_o = V_{DD}/2$, f - Switching frequency

The short circuit current time interval (t_{sc}) can be calculated from Equation (3) and short circuit power is calculated by equation (4).

Sub-Threshold Leakage Power

The NMOS and PMOS transistors used in a CMOS logic gate generally have non- zero sub-threshold and reverse leakage currents. This component of leakage current in CMOS circuits is due to carrier diffusion between the source and the drain regions of the transistor in weak inversion. Figure 7 shows the sources of sub threshold

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current and leakage current. The leakage current is due to reverse biased drain to bulk junctions when the transistors are ON. The sub threshold leakage is due to the reduction in barrier potential along the channel. The leakage current ($I_{leakage}$) of the diode is described by the following Equation (5).

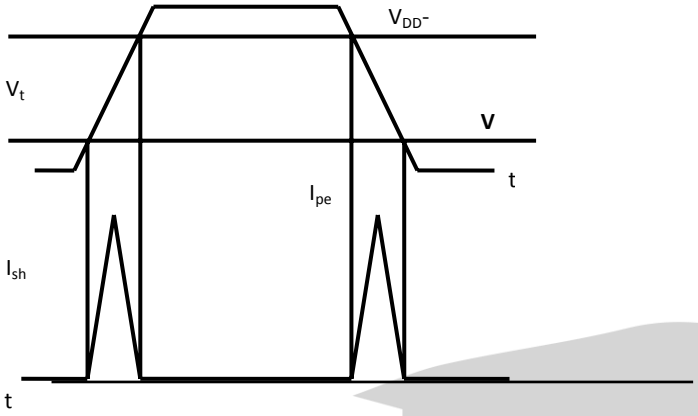

Figure 6 Short circuit current I_{SC} in CMOS capacitor with small C_L

$$I_{leakage} = I_s (e^{qv/kT} - 1) \quad (5)$$

Where I_s = Reverse saturation current V = Diode voltage

k = Boltzmann's constant (1.38×10^{-23} J/K) q = Electronic charge (1.602×10^{-19} C)

T = Temperature (^{0}C)

$$P_{leackage} = (\sum \text{leakage currents}) * \text{supply voltage} \quad (6)$$

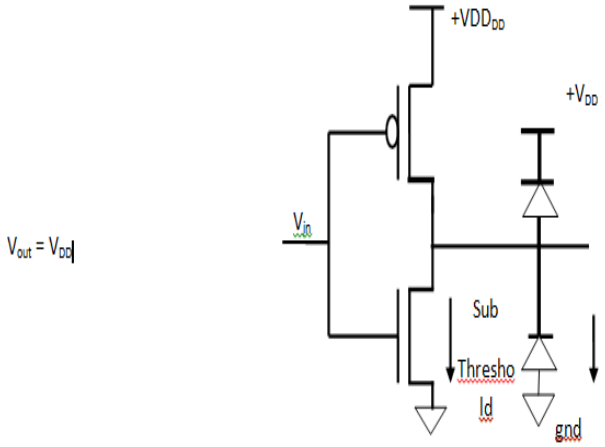

Figure 7 Sub-Threshold current of CMOS inverter

The leakage power $P_{leakage}$ can be calculated using Equation (6). Power Consumption in a CMOS circuit is due to various currents required to charge the load capacitance. In order to reduce power, it is required to reduce the load capacitance, or change the geometries of transistors. However, these techniques would not significantly reduce power consumption. There are various schemes that have been reported and also adopted for power reduction [2]. Next section discusses various low power techniques in CMOS circuits.

II. LOW POWER DESIGN TECHNIQUES

Several low power techniques have been reported in the literature for power reduction. At the gate level and circuit level, power reduction is achieved by incorporating additional logic that can control the charging and discharging of current. David Flynn explained about number of power reduction methods that have been used for some time and are also known as mature technologies [3]. The four power different power reduction techniques are (i) Clock gating (ii) Gate level power optimisation (iii) Multi V_{dd} technique (iv) Multi V_t technique

2.1 DESIGN AND ANALYSIS OF CMOS INVERTER FOR LOW POWER

As the focus of this research work is on design of low power architecture for complex signal and communication applications, it is required to understand the power dissipation at all levels of abstraction. The fundamental building block of a complex VLSI circuit is the inverter; it is required to understand the power dissipation details of an inverter. Hence, an experimental setup is built to estimate the power dissipation aspects of CMOS inverters. This analysis helps in estimating the source of power dissipation and also helps in analyzing the impact of low power techniques in minimizing power dissipation. Based on the discussion presented earlier, CMOS inverter is modeled using Cadence Virtuoso EDA tool, targeting 130 nm Technology. Various sources of power dissipation are estimated based on the experimental setup. Spectre simulation of the experimental setup for power analysis is carried out and the results are presented in next section. Power dissipation in a CMOS circuits depends on various factors such as device geometries, power supply, frequency of operation and load capacitance[4].

III. CALCULATING DYNAMIC POWER DISSIPATION

From low to high input transition period, PMOS transistor switches to ON state and then the current which is flowing from the PMOS will give the total amount of current which represents switching power. This is nothing but the area under the current curve that gives the total current and when multiplied with the supply voltage will give the total switching power. The power dissipations results obtained from experimental setup are shown in Table 1

Table 1 Power dissipations against various Supply voltage source -V_{DD}

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V_{DD} – V	Short circuit power (w)	Switching power (w)	Leakage power (w)	Average power (w)	Peak power (w)
1.8	-1.150 E^{-14}	-1.094 E^{-13}	-1.207 E^{-13}	3.733 E^{-5}	2.659 E^{-4}
2.5	-4.760 E^{-14}	-4.042 E^{-13}	-9.021 E^{-14}	9.280 E^{-5}	5.364 E^{-4}
3.3	-8.156 E^{-14}	-9.876 E^{-13}	-1.409 E^{-12}	2.975 E^{-4}	9.105 E^{-4}

By changing the source voltages we observed that the amount of power obtained is increased. Table2 shows the variation in the power dissipation against the various load capacitances. Table 3 shows various power dissipations versus change in W_n/W_p factor.

Table 2 Power dissipation against variation in the load capacitance

Cload Farads	Short circuit power (w)	Switching power (w)	Leakage power (w)	Average power (w)	Peak power (w)
0.1p	-1.150 E^{-14}	-1.094 E^{-13}	-1.207 E^{-13}	3.733 E^{-5}	2.659 E^{-4}
0.2p	-6.527 E^{-15}	-8.378 E^{-16}	-1.089 E^{-13}	7.221 E^{-5}	3.411 E^{-4}
0.1u	6.1 E^{-14}	2.24 E^{-15}	-9.383 E^{-18}	1.8903 E^{-4}	4.6603 E^{-4}

Table 3 Power dissipations versus W_n/W_p ratio

Wn/Wp ratio	Short circuit power (w)	Switching power (w)	Leakage power (w)	Average power (w)	Peak power (w)
0.5	-1.150 E^{-14}	-1.094 E^{-13}	-1.207 E^{-13}	3.733 E^{-5}	2.659 E^{-4}
0.4	5.1633 E^{-14}	2.24 E^{-15}	-4.83 E^{-17}	3.992 E^{-4}	5.386 E^{-4}
0.2	3.39 E^{-14}	2.24 E^{-15}	-4.83 E^{-17}	1.17 E^{-4}	2.909 E^{-4}

IV. CONCLUSION

As the load capacitance and the V_{DD} increases then the power obtained is also increased. From the analysis carried out the work can be concluded as- "Larger value of load capacitance, higher transistor geometries and higher values of power supply voltage affect the overall power of a CMOS inverter", "Increase in supply voltage reduces short circuit power" and "Leakage power can be reduced by having higher geometries of transistor and higher values of power supply". Analyzing the performances of CMOS inverter helps in understanding the sources of power dissipation.

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