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Circuit Design and Optimization of UBCT Cascode Amplifier

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Abstract - The Unipolar-Bipolar Composite Transistor (UBCT) Cascode Amplifier circuit consists of a UBCT common-source amplifier stage directly coupled to a BJT common-base amplifier stage. Thus the UBCT cascode amplifier combines the advantages of both amplifiers to provide high voltage gain along with wide frequency bandwidth. In the present correspondence, the experimental observations regarding optimization of the circuit components of UBCT cascode amplifier have been precisely analyzed. On the basis of these observations, the best possible performance concerning to the voltage gain of UBCT cascode amplifier has been achieved.

Keywords - Unipolar-Bipolar Composite Transistor, UBCT, UBCT Amplifier, UBCT Cascode Amplifier

I. INTRODUCTION TO UBCT

The Unipolar-Bipolar Composite Transistor (UBCT) embodies the composite circuit of unipolar transistor JFET, bipolar transistor BJT and a pair of resistors. The performance of UBCT is distinctly improved due to unification of high input resistance of JFET and linear transfer characteristics of BJT. The simplified circuit of UBCT is designed with n-channel JFET (BFW10), npn BJT (CL100) & source-emitter resistor pair (R_S-R_E) and it is enclosed as a three terminal device as depicted in fig.1 [1].

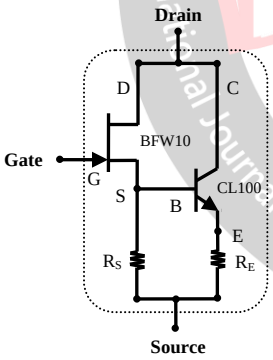

Fig.1. Circuit Design of UBCT

The circuit components of UBCT are experimentally optimized to achieve the best possible performance [2]. The static characteristics of UBCT show transfer curve linearity along with high input resistance [3]. According to the dynamic characteristics, the drain resistance and transconductance curves also exhibit linear performance over a wide range of drain-to-source voltage and gate-to-source voltage respectively up to the pinch-off voltage of UBCT [4]. Thus the enhanced dynamic performance of UBCT promotes its application as an efficient amplifier in common-source (CS) mode [5]. The experimental analysis of the variants of UBCT CS amplifier reflects that the best result is obtained by a typical UBCT having JFET (BFW10), BJT (CL100) and source-emitter resistor pair (R_S-R_E) (100Ω-10Ω) [6]. In the power budget estimation of UBCT CS amplifier, the peak of voltage gain to total power dissipation ratio appears at the supply voltage of 18V with an efficiency of 0.066dB/mW [7]. This variant of UBCT CS amplifier offers frequency bandwidth of 1MHz with maximum voltage gain of 13.77dB and 2MHz with maximum voltage gain of 8.85dB for the supply voltage of 18V and 15V respectively [8]. Therefore, the UBCT CS amplifier exhibits good power efficiency, moderate voltage gain and wide frequency bandwidth.

II. CIRCUIT DESIGN OF UBCT CASCODE AMPLIFIER

The UBCT cascode amplifier is a two-stage amplifier circuit which consists of a UBCT common-source (CS) amplifier stage directly coupled to a BJT common-base (CB) amplifier stage. As depicted in fig.2, UBCT cascode amplifier circuit comprises a typical variant of UBCT [JFET (BFW10), BJT (CL100) & source-emitter resistor pair (R_S-R_E) (100Ω-10Ω)] as active component in UBCT CS amplifier and an additional BJT (CL100) as CB amplifier. The UBCT CS amplifier circuit is connected in self-biased topology and the BJT CB amplifier circuit in voltage-divider biased topology to achieve better stability. The UBCT cascode amplifier combines the advantages of high input impedance of UBCT CS amplifier as well as high output impedance, high voltage gain and high frequency performance of BJT CB amplifier [9]. In the UBCT cascode amplifier circuit, the UBCT CS stage provides high input impedance with low voltage gain to ensure the reduction in input Miller capacitance. Thus the minimization of Miller capacitance-gain multiplication effect offers expansion in operating frequency bandwidth. Also, because of high voltage gain provided by the BJT CB

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stage, the overall voltage gain of UBCT cascode amplifier becomes high [10]. Therefore, the UBCT cascode amplifier circuit is designed to achieve high voltage gain along with wide frequency bandwidth.

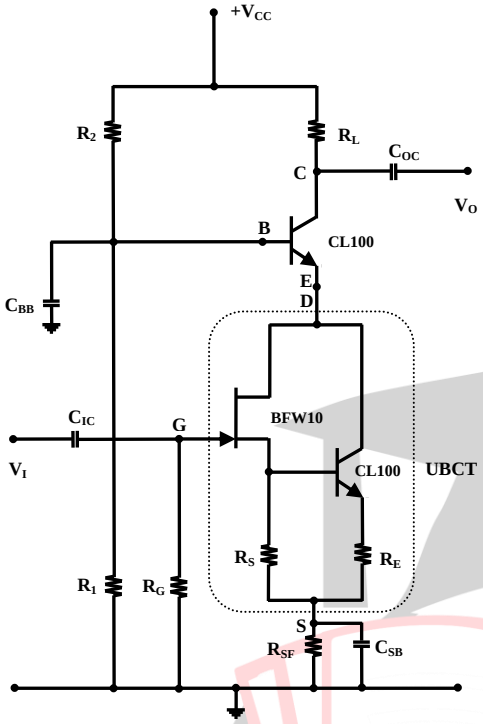

Fig.2. Circuit Design of UBCT Cascode Amplifier

III. CIRCUIT OPTIMIZATION OF UBCT CASCODE AMPLIFIER

To obtain the optimal circuit of UBCT cascode amplifier for attaining the maximum voltage gain involves experimental investigation of circuit components regarding optimization of BJT biasing resistor pair (R_1-R_2), load resistor (R_L), source feedback resistor (R_{SF}), base bypass capacitor (C_{BB}) and source bypass capacitor (C_{SB}) for a particular range of supply voltage (V_{CC}) within the operating temperature range of 30°C-33°C. The value of gate resistor R_G should be large (typically of 1MΩ) to keep the gate voltage at approximately zero and also to prevent loading of the ac signal source [11]. The input coupling capacitor (C_{IC}) and the output coupling capacitor (C_{OC}) are also kept at large value (typically of 10µF) to provide ac short circuit condition at the operating frequency and to block DC so as not to disturb the biasing condition [12]. Therefore, the gate resistor R_G=1MΩ and the input & output coupling capacitors C_{IC}=C_{OC}=10µF are initially kept constant. For input signal, ac voltage (sine wave) of 100mV (peak-to-peak) having constant frequency of 1kHz is applied to the UBCT cascode amplifier circuit.

(a) Optimization of BJT Biasing Resistor Pair (R_1-R_2)

The fig.3 depicts the voltage gain with negative feedback A_{VF} versus the supply voltage V_{CC} of UBCT cascode amplifier for different BJT biasing resistor pairs (R_1-R_2) having values (2.2kΩ-10kΩ), (4.7kΩ-10kΩ) and (10kΩ-10kΩ). The BJT biasing resistor pairs (R_1-R_2) (4.7kΩ-10kΩ) and (10kΩ-10kΩ) perform better as the voltage gain of 12.71dB and 7.78dB have been achieved respectively for the supply voltage V_{CC}=15V. Also at V_{CC}=21V, BJT biasing resistor pairs (R_1-R_2) (4.7kΩ-10kΩ) and (10kΩ-10kΩ) attain higher voltage gain of 14.80dB and 13.74dB respectively. For full range of supply voltage, the BJT biasing resistor pair (R_1-R_2) (2.2kΩ-10kΩ) offers low voltage gain. Thus the UBCT cascode amplifier achieves the best performance by using the BJT biasing resistor pair (R_1-R_2) (4.7kΩ-10kΩ) having voltage gain of 12.71dB, 14.07dB and 14.80dB for the supply voltage of 15V, 18V and 21V respectively. Since a little increment in voltage gain is observed with increase in supply voltage from 18V to 21V for the BJT biasing resistor pair (R_1-R_2) (4.7kΩ-10kΩ), hence the optimized value for the supply voltage is assumed to be 18V.

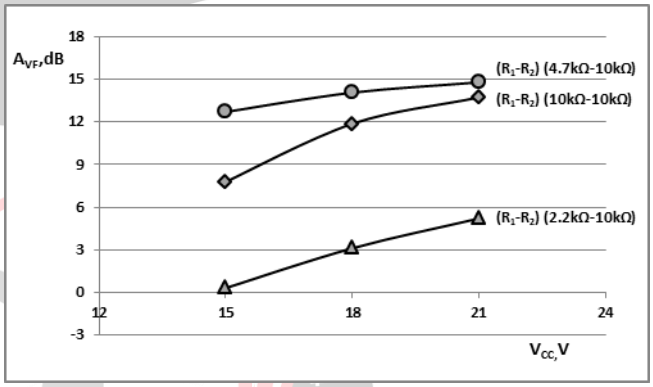

Fig.3. Voltage gain with negative feedback A_{VF} of UBCT Cascode Amplifier versus Supply Voltage V_{CC} for different BJT Biasing Resistor pair (R_1-R_2)

[Circuit specifications: UBCT [JFET BFW10, BJT CL100 and source-emitter resistor pair (R_S-R_E) (100Ω-10Ω)], BJT CL100, R_G=1MΩ, R_L=1kΩ, R_{SF}=100Ω, C_{IC}=C_{OC}=10µF, C_{BB}=10µF, C_{SB}=N/C].

(b) Optimization of Load Resistor (R_L)

The fig.4 depicts the voltage gain with negative feedback A_{VF} versus the load resistor R_L of UBCT cascode amplifier at constant supply voltage V_{CC} of 18V.

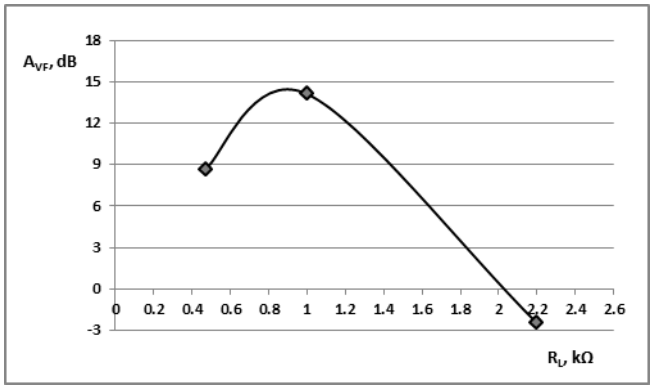

Fig.4. Voltage gain with negative feedback A_{VF} of UBCT Cascode Amplifier versus Load Resistor R_L

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[Circuit specifications: UBCT [JFET BFW10, BJT CL100 and source-emitter resistor pair (R_S-R_E) (100Ω-10Ω)], BJT CL100, BJT biasing resistor pair (R_1-R_2) (4.7kΩ-10kΩ), R_G=1MΩ, R_{SF}=100Ω, C_{IC}=C_{OC}=10μF, C_{BB}=10μF, C_{SB}=N/C].

By varying load resistor R_L from 470Ω to 2.2kΩ, the maximum voltage gain of 14.13dB is obtained for the load resistor of 1kΩ. The voltage gain increases from 8.69dB to 14.13dB with increase in load resistor from 470Ω to 1kΩ and thereafter, the voltage gain decreases up to -2.50dB for load resistor of 2.2kΩ. Thus the load resistor R_L of 1kΩ exhibits much improved voltage gain with respect to 470Ω and 2.2kΩ.

(c) Optimization of Source Feedback Resistor (R_{SF})

The fig.5 depicts the voltage gain with negative feedback A_{VF} versus the source feedback resistor R_{SF} ranging from 10Ω to 1kΩ at constant supply voltage V_{CC} of 18V. The five different source feedback resistors R_{SF} having values 10Ω, 100Ω, 220Ω, 470Ω and 1kΩ show the voltage gain of 3.08dB, 14.08dB, 13.52dB, 4.19dB and 1.05dB respectively. Thus the peak value of voltage gain is observed at 14.08dB with source feedback resistor R_{SF}=100Ω.

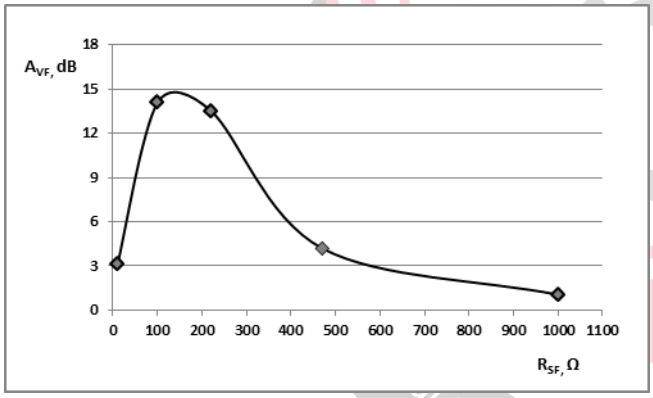

Fig.5. Voltage gain with negative feedback A_{VF} of UBCT Cascode Amplifier versus Source Feedback Resistor R_{SF}

[Circuit specifications: UBCT [JFET BFW10, BJT CL100 and source-emitter resistor pair (R_S-R_E) (100Ω-10Ω)], BJT CL100, BJT biasing resistor pair (R_1-R_2) (4.7kΩ-10kΩ), R_G=1MΩ, R_L=1kΩ, C_{IC}=C_{OC}=10μF, C_{BB}=10μF, C_{SB}=N/C].

(d) Optimization of Base Bypass Capacitor (C_{BB})

The fig.6 depicts the voltage gain with negative feedback A_{VF} versus the base bypass capacitor C_{BB} ranging from 0.01μF to 10μF at constant supply voltage V_{CC} of 18V. A little increment in voltage gain from 13.30dB to 14.10dB is noticed with increase in base bypass capacitor from 0.01μF to 10μF. The voltage gain of the amplifier depends on the value of base bypass capacitor but in the cascode circuit, the base terminal of the BJT CB amplifier must be ac grounded by a high value of base bypass capacitor. Thus the base bypass capacitor C_{BB}=10μF is recommended.

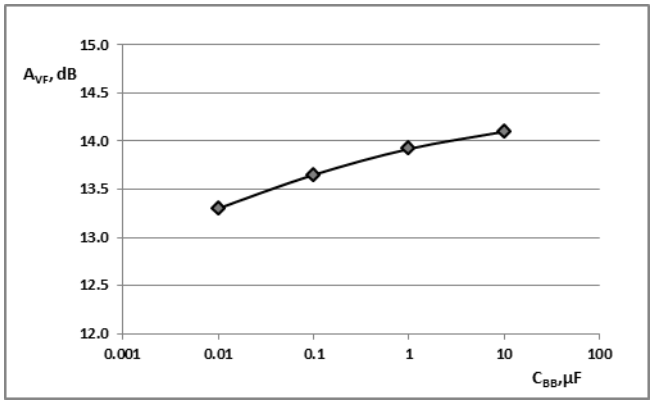

Fig.6. Voltage gain with negative feedback A_{VF} of UBCT Cascode Amplifier versus Base Bypass Capacitor C_{BB}

[Circuit specifications: UBCT [JFET BFW10, BJT CL100 and source-emitter resistor pair (R_S-R_E) (100Ω-10Ω)], BJT CL100, BJT biasing resistor pair (R_1-R_2) (4.7kΩ-10kΩ), R_G=1MΩ, R_L=1kΩ, R_{SF}=100Ω, C_{IC}=C_{OC}=10μF, C_{SB}=N/C].

(e) Optimization of Source Bypass Capacitor (C_{SB})

The fig.7 depicts the voltage gain without feedback A_V versus the source bypass capacitor C_{SB} ranging from 0.01μF to 10μF at constant supply voltage V_{CC} of 18V. The voltage gain increases from 14.28dB to 22.04dB with increase in source bypass capacitor C_{SB} from 0.01μF to 10μF. The four different source bypass capacitors C_{SB} having values 0.01μF, 0.1μF, 1μF and 10μF show the voltage gain of 14.28dB, 14.49dB, 16.09dB and 22.04dB respectively. Since the voltage gain of the amplifier depends on the value of source bypass capacitor, hence the value of component should be selected as per the requirement of circuit application. The source bypass capacitor is used to keep the source terminal of UBCT at ac ground for the operating frequency. Thus the application of source bypass capacitor C_{SB} violates the negative feedback process and improves the voltage gain without feedback.

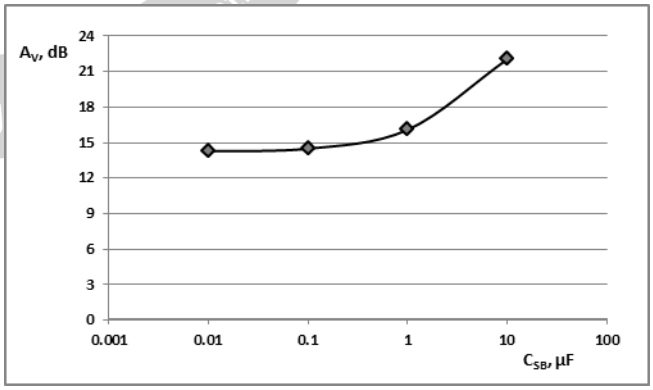

Fig.7. Voltage gain without feedback A_V of UBCT Cascode Amplifier versus Source Bypass Capacitor C_{SB}

[Circuit specifications: UBCT [JFET BFW10, BJT CL100 and source-emitter resistor pair (R_S-R_E) (100Ω-10Ω)], BJT CL100, BJT biasing resistor pair (R_1-R_2) (4.7kΩ-10kΩ), R_G=1MΩ, R_L=1kΩ, R_{SF}=100Ω, C_{IC}=C_{OC}=10μF, C_{BB}=10μF].

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IV. CONCLUSION

The properly designed UBCT cascode amplifier provides voltage gain with negative feedback A_{VF} of 14.07dB and 14.80dB for supply voltage V_{CC} of 18V and 21V respectively with optimized value of circuit components as BJT biasing resistor pair (R_1-R_2) (4.7kΩ-10kΩ), load resistor R_L=1kΩ, source feedback resistor R_{SF}=100Ω and base bypass capacitor C_{BB}=10µF. The gate resistor R_G=1MΩ and input & output coupling capacitors C_{IC}=C_{OC}=10µF are initially kept constant. The source bypass capacitor C_{SB} may be connected in the circuit if higher voltage gain without feedback is required as per the circuit application. On the basis of these observations, the best possible performance concerning to the voltage gain of UBCT cascode amplifier has been achieved.

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