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Design and Analysis of Different Types of Full Adder Circuits

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Abstract: In many processing systems especially in digital signal processing the full adders are the main component In Multipliers to add the partial products full adders are used. To decrease the power consumption, decreasing the number of transistor count in full adder is a solution. Different types of full adders are implemented in this paper by using cadence virtuoso 180nm and 90nm technology to reduce the total power consumption of full adder.

Keywords: Full adder, Pass Transistor logic (PTL), GDI, 28T, 20T, 14T.

I. INTRODUCTION

Low power VLSI is the main constrains in current days due to increase of low power devices and high speed processing systems. The multipliers are introduced to overcome this problem. To multiply the two binary numbers Multipliers are used. The partial products will be generated by multiplier circuit and the adder circuit i.e. full adder circuit is used to add these partial products. In the multiplier block the 1-Bit full adder cell is the main building block [7]. The full adder is consists of three inputs A, B, C_{in} and two outputs sum and carry. [1] The sum is given as SUM = A ex-or B ex-or C_{in} and carry is given as CARRY = AB + BC + CA. The block diagram of the full adder is given in figure1.

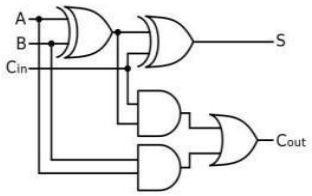

Figure 1: Full adder Block Diagram

The truth table for full adder is given below

A	B	C_{in}	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

So, the main focus is going on how to decrease the total number of transistor count in a full adder. There are many techniques has been introduced to reduce the number of transistors in full adder like Dynamic and domino Cmos logic, Gate Diffusion Input (GDI), Pass Transistor Logic (PTL).[2]

II. DIFFERENT TYPES OF FULL ADDERS

The different types of full adders have been discussed in this section. There are different types of full adders present like Conventional full adder with 46T, 28T, 20T, 14T, 8T and 6T.

Conventional 46 T Full adder: The conventional full adder is designed with the help of two half adder circuits along with one OR gate. The half adder circuit is consists of one x-or gate and one AND gate [3]. The block diagram of the conventional 46T full adder is shown in figure 2.

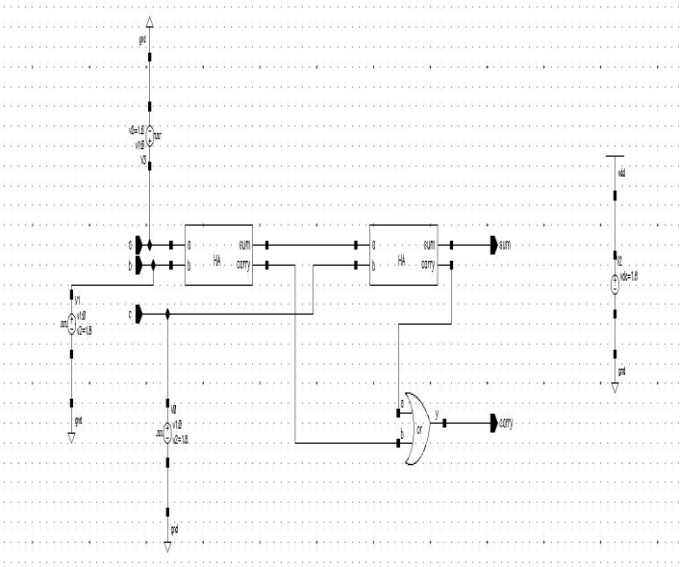

Figure 2: Conventional 46T Full adder

In this full adder, the number of transistor count is 46. High power consumption can be occurs in this type of full adder because of more number of transistors. So, we need to decrease the total number of transistor count. In order to reduce the total number of transistors we go for the reducing the expression of sum and carry using demorgan's theorem.

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28 T Full adder Circuit: The 28 number of transistors can be used to design 28T full adder circuit we use to perform the full adder function. This technique produces the less delay and low power consumption as compared to 46T full adder[4]. The block diagram for 28T full adder is given in figure 3.

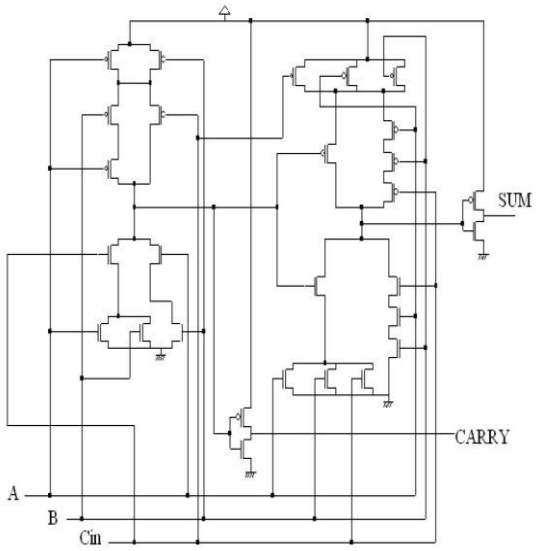

Figure 3: 28T full Adder

20T full adder circuit: To design the full adder here we use total 20 numbers of transistors which acts as a full adder. The total number of transistors reduced again so the total power consumption and delay can be reduced of the full adder circuit [4]. The circuit diagram of 20T full adder is given in figure 4.

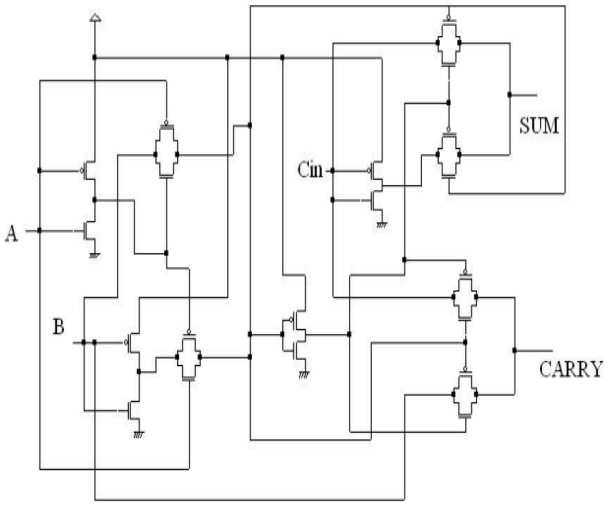

Figure 4: 20T Full Adder

14T Full adder Circuit: with the help of EXOR- EXNOR the 14T full adder is designed and it is designed with 14 transistors. Due to high voltage swing present if 14T full adder will consumes more power than the other full adder designs [5] [6]. The structure of 14T is given in figure 5.

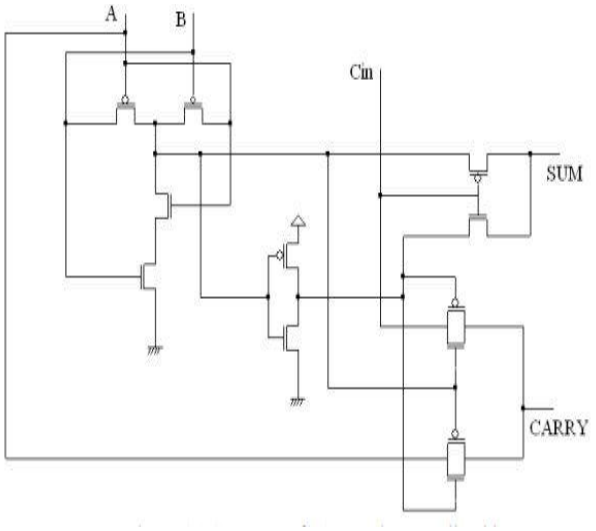

Figure 5: Block diagram of 14 T Full Adder

III. IMPLEMENTATION

The 46T full adder simulation results of the conventional full adder are given in figure 6.

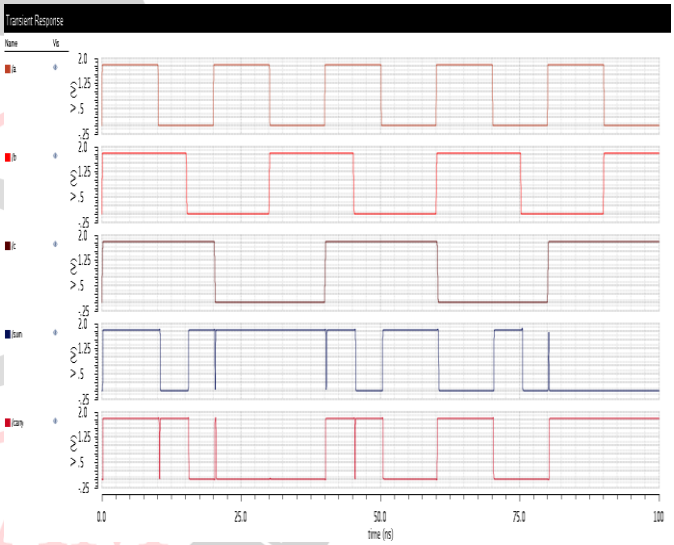

Figure 6: Output waveforms of 46T Full Adder

The 28T full adder output wave forms are shown in figure 7.

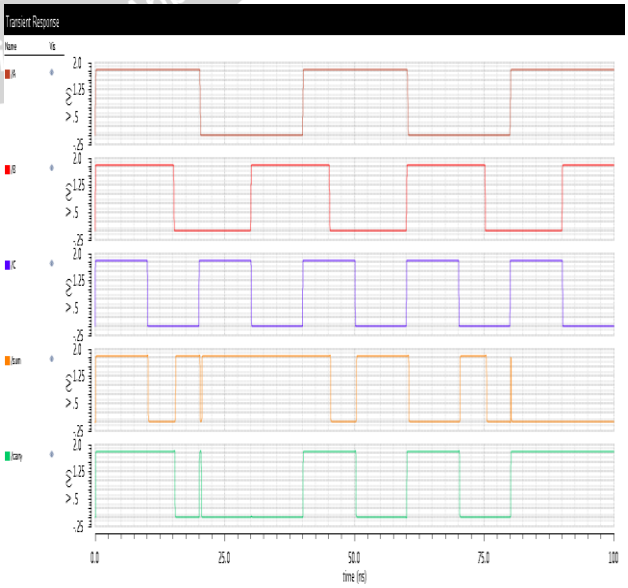

Figure 7: Output waveforms of 28T Full Adder

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The 20T full adder output waveforms are shown in figure 8.

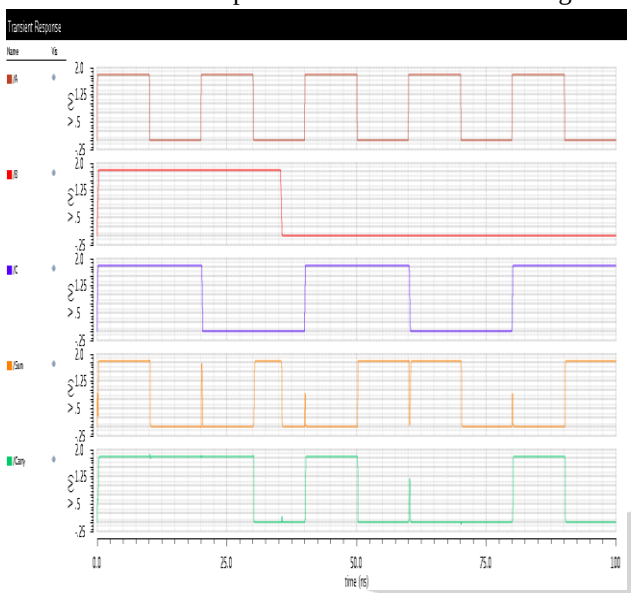


Figure 8: Output waveforms of 20T Full Adder

The 14T full adder output waveforms of are shown in figure 9.

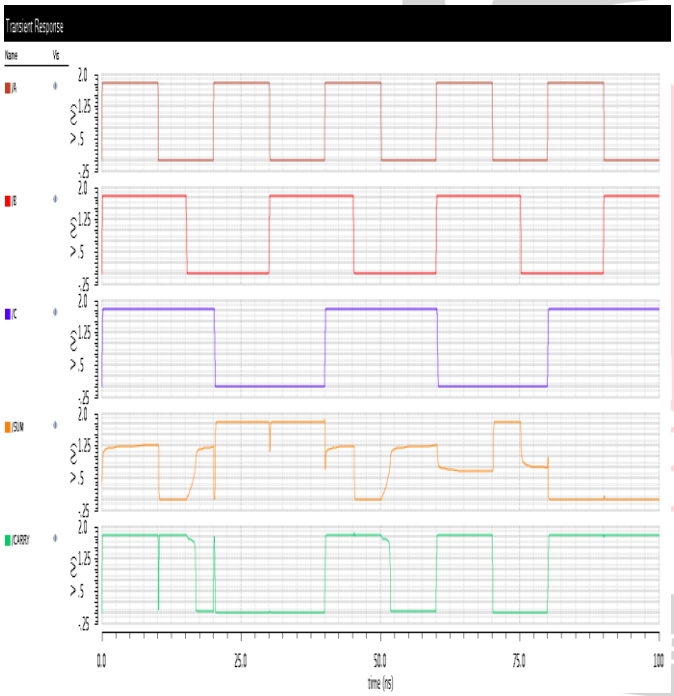


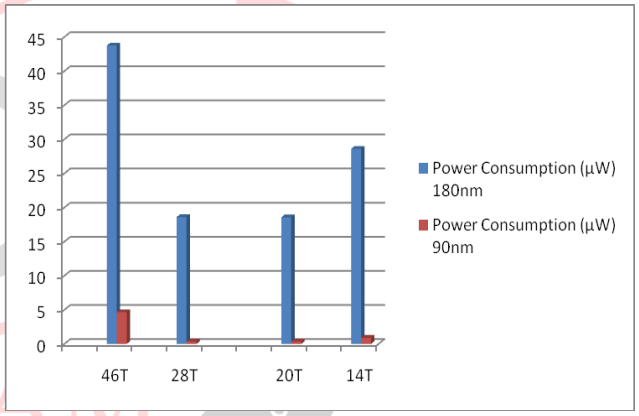
Figure 9: Output waveforms of 14T Full Adder

Table 1 Comparison table of power consumption by different types of full adders in 180nm Technology.

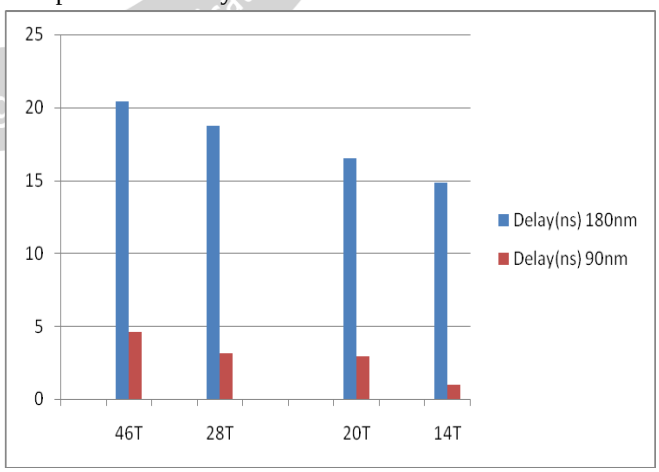
Full Adder	Power Consumption (µW)		Delay(ns)	
	180nm	90nm	180nm	90nm
46T	43.74	4.651	20.4	4.58
28T	18.59	0.3454	18.7	3.12
20T	18.56	0.3568	16.5	2.92
14T	28.6	0.8926	14.8	0.98

In the above table we compared the total power consumption and delay of the different types of full adders and first we found that the total power consumption of a full adder is much lesser in 20T full adder design using 180nm technology and after applying 90nm technology the total power consumption is decreased as compared to 180nm for the same 20T full adder design but the in the next design i.e. 14T full adder even though the number of transistors are decreased but the power consumption is much higher as compared to 20T full adder design this is due to high voltage swing in 14T design and next we calculated the delay of the circuit which can cause the speed of the circuit and we found that the 14T full adder design is getting much lesser delay as compared to all the other design in both 180nm and 90nm technology but using 90nm technology the delay is much lesser.

Comparison of Power consumption



Comparison of Delay



IV. CONCLUSION

In this paper the power consumption and delay of all the different types of full adder circuits are determined and calculated. The full adder cell is the basic building block of

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the many applications of multipliers. According to the results, the power consumption in 20T full adder is 18.59 µW in 180 nm technology and 0.3568 µW in 90nm technology which is much lesser as compared all the other designs in 180nm and 90nm technology but the delay in 14T full adder is 14.8ns in 180nm technology and 0.98ns in 90nm technology which is much lesser as compared to other designs But in the 14T full adder, the transistor count is less but power consumption is more due to the high output swing but 14T full adder is having much better power delay product compared to all the other full adder designs. In future the total number of transistors can be reduced by opting the new techniques and by reducing the nano meter technology.

V. REFERENCES

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