Design of Quadratic Equations Multiplier using Urdhava Triyakbhayam Sutra of Vedic Mathematics

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Abstract Vedic mathematics is the most proficient alternative to conventional mathematics as it simplifies and converts larger computation to smaller one. Vedic Algorithm can also be applied on Binary Arithmetic operations also. In this paper Urdhava Triyakbhayam sutra of Vedic Mathematics is used to implement the multiplication of two quadratic equations. This paper proposes a design for multiplication of two quadratic equations having 2 bit coefficients. Proposed multiplier is designed in VHDL, synthesized and simulated using Xilinx Synthesis Tool ISE 8.1.Power consumption of the circuit is measured using xpower tool.

Keywords — Quadratic equation, Urdhava Triyakbhyam sutra, Vedic multiplier, VHDL, VLSI, Xilinx.

I. INTRODUCTION

With advances in the VLSI technology hardware implementation has become an attractive alternative. Assigning complex computation tasks to hardware and exploiting the parallelism and pipelining in algorithms yield significant speed up in running times. Moreover, computers may be getting faster but there are always new applications that need more processing speed from earlier. To meet the present and future demanded applications, modern techniques (algorithms) for accelerating applications on hardware need to be developed. The polynomial functions are required in many applications. Implementation of pipelined polynomial functions will help in many practical applications such as Curve fitting , Estimating functions such as SIN, COS, ATAN, Logarithmic functions and Exponential functions.

Vedic Mathematics was reconstructed from Vedas. The whole Vedic mathematics is based on 16 sutra providing unique and simple techniques to various mathematics computations. The Vedic algorithms are equally suited for binary platforms providing improvement to various design parameters for computing arithmetic operations [1]. Vedic mathematics can also be applied for the multiplication of two quadratic equations.

In this paper a design for the multiplication of two quadratic equations has been proposed which is based upon the Urdhava Triyakbhayam sutra of Vedic mathematics. The proposed design is efficient in terms of hardware as compared to the design proposed in [2].

This Paper is structured as Follows: Section II briefly introduce Urdhava Triakbhyam sutra.Section III reprsents the Schematics of 2x2 bit quadratic equation multiplier designed using urdhava Triyakbhyam sutra and their waveforms. Section IV shows the simulation results of device utilization, Power Dissipation, Delay and memory utilized of these designs. Finally Section V comprises of conclusion.

II. URDHVA TIRYAKBHYAM SUTRA

Urdhva tiryakbhayam sutra is a general multiplication formula applicable to all cases of multiplication [2]. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products.

A lot of research work have been carried out on vedic mathematics algorithms**.** In [4] the general technique for NxN multiplication is proposed using Urdhvatrayagbhayam Sutra. For the addition of partial products generated carry look ahead adder is used. In [5] the authors concludes that Urdhva tiryakbhyam, being general mathematical formula, is equally applicable to all cases of multiplication. Due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. This problem has been solved by introducing Nikhilam Sutra. The architecture for a 16×16 Vedic multiplier module based upon Urdhva Tiryagbhyam Sutra and "Nikhilam Sutra" technique using Carry save adder is shown in [6]. The author in [7] proved that Vedic mathematics based DSP requires less processing time than inbuilt MATLAB functions, Gives better result. The author in [8] presented the VLSI Architecture for High-Speed 32-bit Multiplier using Nikhilam Sutra and Urdhva-Tiryagbhyam Sutra. The concludes that as the number of bits increases delay can be

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reduced by using Urdhva-tiryagbhyam Vedic multiplier with BEC-1 adders. In [9] authors proposed the design of a 2-bit multiplier for multiplying two quadratic equations using Vedic Technique 'Urdhva Tiryakbhyam' at 180nm cmos. The power consumption of the design has been measured. The architecture of quadratic equation multiplier proposed in [9] is given in Fig.2.

The parallelism in generation of partial products and their summation is obtained using Urdhava Triyakbhyam explained in fig 1.To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (225 * 316). The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

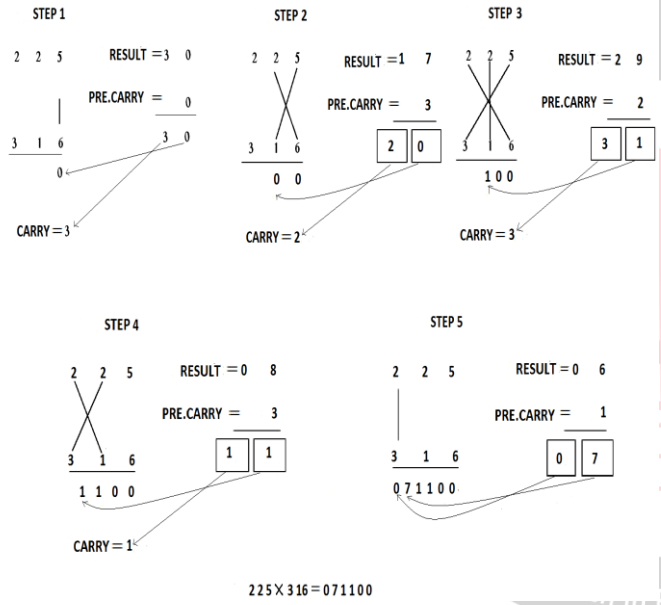

Fig.1 Multiplication of two decimal numbers by Urdhva Tiryakbhyam

III. 2X2 BIT QUADRATIC EQUATION MULTIPLIER

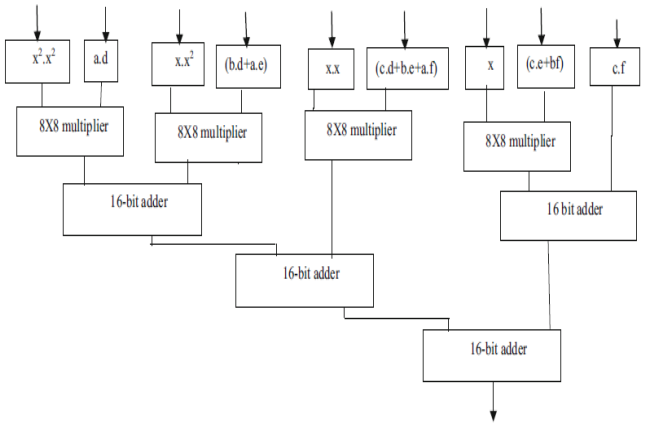

Fig. 2 2x2 bit Quadratic Equation Multiplier Architecture Proposed in [9]

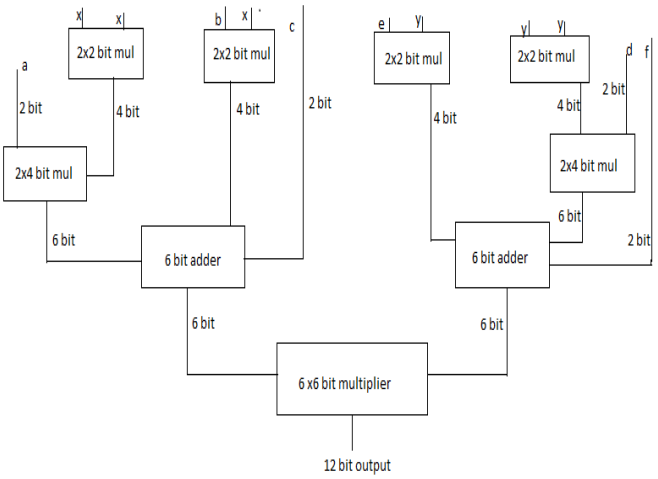

Fig.3 Modified Architecture of 2x2 bit quadratic equation multiplier

The above shown Fig.3 consists of the methodology for the multiplication of two quadratic equations ax^2+bx+c and dy^2+ey+f. This is the modified architecture and is hardware efficient as proposed in [9].This multiplier is designed for the multiplication of quadratic equations where the coefficient a,b,c,d,e,f,and variable x,y all are up to 2bits.The 2x2 bit multipliers, 2x4 bit multiplier and 6x6 bit multipliers are designed using Vedic mathematics. 6x6 bit multiplier is designed by using 3x3 bit multipliers. All the multipliers used here are based upon urdhava triyakbhayam sutra. VHDL coding is done for the above design and simulated using Xilinx ISE tool. Fig,4 shows the RTL schematic of the multiplier. For VHDL coding structural modeling is used. So 3x3 bit multiplier is used as a component in 6x6 bit multiplier. 2x4 bit multiplier is designed by using two 2x2 bit multipliers.

The methodology for the multiplication of the two quadratic equations is explained below. Here all the coefficient and variables are of 2 bit :

- Compute x^2 by using 2x2 bit multiplier. X is 2 bit. This 2x2 bit multiplier gives 4 bit output.
- Compute ax^2 by 2x4 bit multiplier. It gives 6 bit output.
- Multiply b and x by using 2x2 bit multiplier. The output will be 4 bit.
- Now add the terms calculated above ax^2, bx and c by using 6 bit adder. The output will be 6 bit.
- Similarly computes dy^2+ey+f.The output will be 6 bit
- Now multiply the results by using 6x6 bit vedic multiplier as shown in Fig.4. The final result will be 12 bit.

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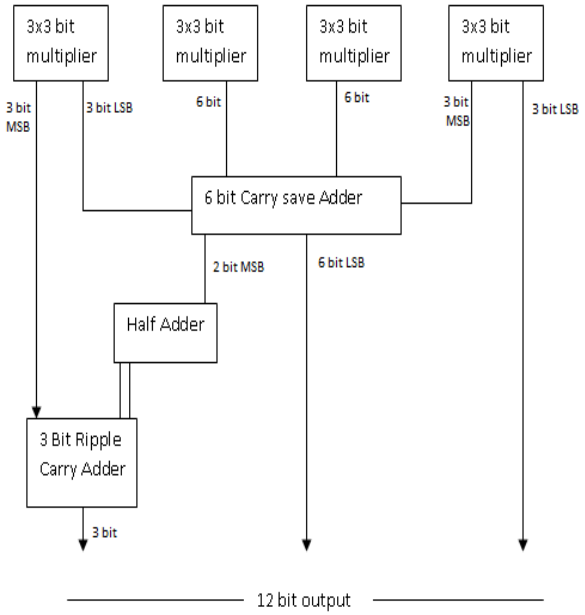

Fig. 4 6x6 bit vedic multiplier

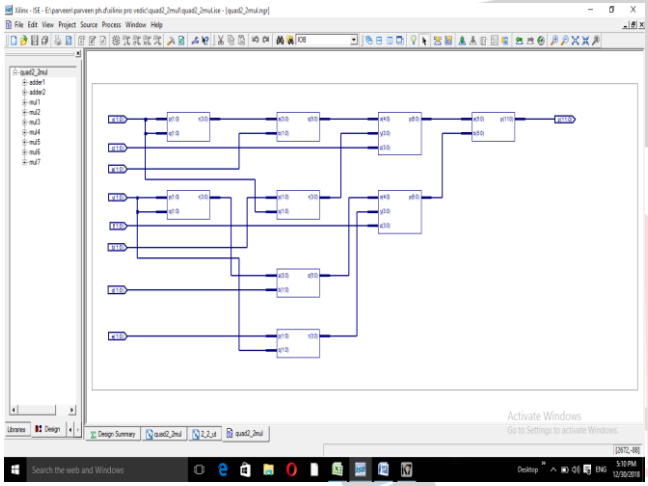

Fig.5 RTL schematic of 2x2 bit quadratic equation multiplier.

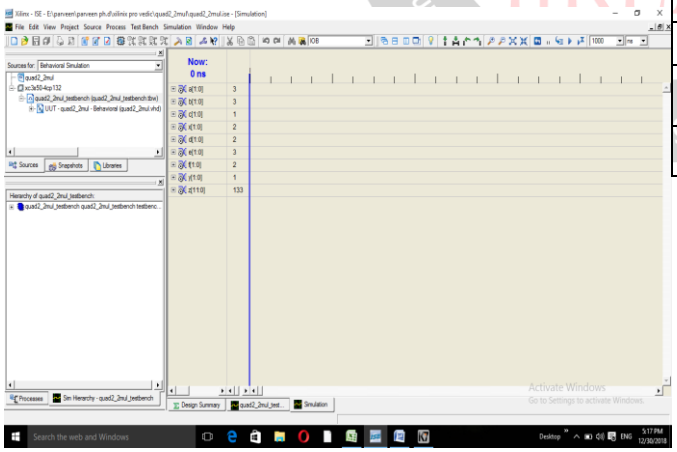

Fig.6 Simulation waveform of 2x2 bit quadratic equation multiplier

IV. SIMULATION RESULTS

The Performance of the proposed multiplier is evaluted based on their Area, Power dissipation, Delay and memory utilized. All the multipliers used as a component of quadratic equation multiplier are based upon Urdhava triyakbhayam sutra. Because the multipliers based upon this vedic mathematics sutra are efficient in terms of delay and area. All the simulations are performed using Xilinx ISE 8.1i. . Power dissipation of the multipliers is measured using Xpower tool at different frequencies & supply voltages as mentioned in TableI. VHDL descriptions of the multiplier have been implemented using spartan3 Xc3s50cp132-4 and virtex4 XC4VLX100ff1148-10 devices. Power dissipation of the circuit is measured using xpower tool of Xilinx. Power dissipation is measured by applying inputs at 20Mhz and 50 Mhz frequency. Power dissipation is also measured at three input voltage levels 1v,1.2v and 1.8v for analyzing the effect of supply voltage and input frequency on the power dissipation. The proposed design shows less power dissipation on virtex 4.Delay is also less at virtex4 as compared to spartan3 devices. As the frequency of input signal increases the multiplier shows more power dissipation. The area of the multiplier can be further reduced using the different architectures for Vedic multipliers proposed in the literature[8].

Table1. Simulation results

Device	Spartan3	Virtex4
No. Of Slices	71	
No. Of 4 Input LUTs	126	
No. Of Bonded IOBs	28	
DELAY(ns)	31.525ns	18.700ns
Memory Utilized	177408 kilobytes	367680 kilobytes
Power Dissipation (mw)AT (20 Mhz 1v)	19	19
AT (20MHZ,1.2V)	20	19
AT (20MHZ 1.8V)	22	21
AT (50HZ,1V)	21	20
AT (50MHZ,1.2V)	23	21
AT (50MHZ,1.8V)	29	26

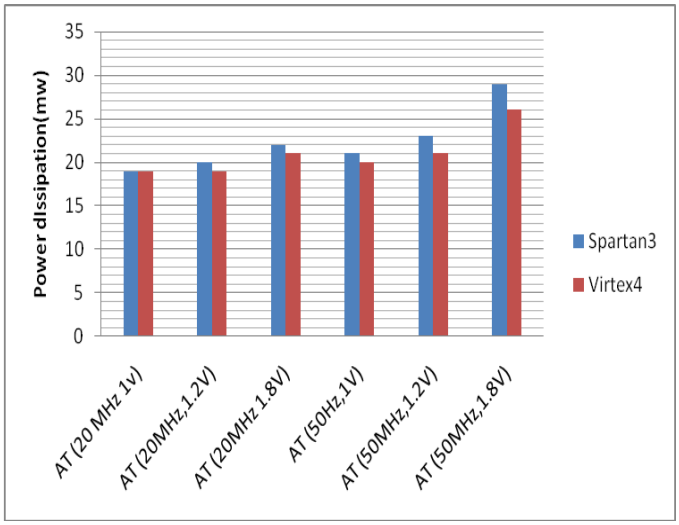

Fig. 7 Power Dissipation (2x2 bit quadratic equation multiplier)

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V. CONCLUSION

This paper presents new architecture for 2x2 bit quadratic equation multiplier. The presented design is efficient in terms of the hardware used as compared to the architecture proposed in [9]. The design is for the multiplication of equation with unsigned constants and variables. The proposed architecture gives minimum delay of 18.7 ns at virtex4 and power dissipation of 19mw at 20Mhz frequency of input signal with 1v supply voltage. Quadratic equation multiplier with Signed number multiplication will be the future work.

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