Implementation Of VLSI Design For High Performance Vedic Multiplier

[1]Abhilash J.E.N, [2]Yagna B, [3]Suresh E, [4]Pavani B, [5]Ravi Teja G

[1]Associate Professor, [2,3,4,5]U.G Students, Department of ECE, Swarnandhra College of Engineering and Technology, Seetharampuram, Andhra Pradesh India.

[1]abhilash.jen@gmail.com, [2]Yagnasatya7@gmail.com , [3]sureshelluri1@gmail.com,

[4]kavyabora777@gmail.com, [5]deviravitejagollu143@gmail.com.

Abstract- Today, in digital circuits, many multipliers have been replaced by high-speed Vedic multipliers using techniques in the Ancient Mathematics of the Vatican of India. Vedic mathematics are an ancient mathematical system that has a unique computer technology based on 16 sutras. This project would demonstrate the effectiveness of the Vedic Urdhva Triyagbhyam-(Vertically and Crosswise) approach to multiply the difference in the same multiplication process. It allows the same generation of intermediate products to eliminate unwanted additions to the zero and higher levels used with the Karatsuba algorithm with different data types. Urdhva tiryagbhyam Sutra is the best Sutra (Algorithm), which provides the least amount of delay to multiply all kinds of numbers. In addition, the coding of Verilog HDL from Urdhva tiryagbhyam Sutra for the development and implementation of 32x32 pieces for Xilinx synthesis tools.

In the current Vedic multiplier architecture, the compiler rescue is now included to increase its performance, we replace it with a parallel high-prefix additive named Koggestone additive. We have observed that the total area decreased by 26% and the productivity of the area also decreased to 16%.

Terms of the index: vedic mathematics, urdhva triyagbhyam sutra, karatsuba algorithm.

I. INTRODUCTION

Increasing is a vital fundamental task in arithmetic operations. Multiplication-based operations such as Many MACs and internal products are among the most commonly used Digital Signal Processing (DSP) applications such as CIAF, Fast Fourier Transform (FFT), Filtering and Microprocessors in Arithmetic and Logic Units [1]). Since multiplication dominates the execution time of most DSP algorithms, a high speed multiplier is required. Currently, multiplication time is a dominant factor in determining the duration of a DSP chip.

The increase in high speed processing has led to the expansion of computer processing and signal processing applications. The higher arithmetic operations are to achieve the desired performance of many real-time signals and image processing applications [2]. One of the key arithmetic operations in these applications is the increase and development of the easy multiplier circuit has become a topic of interest for decades. Decreasing consumption of time and energy consumption is very important for many applications [2,3]. This work demonstrates the various multiplier architectures. The multiplier based on Vedic Mathematics is one of the powerful and low-power multipliers. The reduction of energy consumption for digital systems includes the optimization of all levels of design. The optimization includes the technology used in the implementation of digital circuits, the design of circuits and the topology, the architecture of the circuit and the highest level of algorithms implemented. Digital multipliers are the most commonly used components of any digital circuit design. They are fast, reliable and effective components used to enforce any operation. Depending on the ingredients of the ingredients, there are different types of multipliers available. Specific architectural multipliers are selected based on the application.

In many DSP algorithms, the multiplier is in the critical delay path, and finally determines the algorithm. The speed of operation of the multiplication is very important for the DSP as well as for the general processor. Throughout the year, generalization has become widespread with a single operation of extension, cutting and operation. There are many research algorithms for multiplication, which each offers different advantages and has a compensation in the area of acceleration, breakdown of the circuit, location and energy consumption.

The multiplier is a huge block in the computer system. The number of circuits involved directly proportional to the square in its resolution, that is, a size multiplier n has ports n2. For multiplication algorithms made by latency and production of DSP applications, there are two major concerns about the perspective view. Latency is the true value of calculating a function, a measure of how long the inputs are in a stable state, the final result in outputs.

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Performance is the measure of how many times the multiplication can take; The multiplier is not only a long-term suffering, but also an important source of power failure. Therefore, if it is also intended to maximize energy consumption, it is very important to reduce the deprivation by using various optimization of delay.

Digital multipliers are the basic components of all digital signal processors (DSPs), and the DSP speed is multiplied by the speed of the multiplier [11]. The two most common multiplication algorithms followed by digital hardware are the addition of multiplication algorithms and the Booth multiplication algorithm. The computational time taken by the multiplier of the field is not much, since partial products are calculated independently simultaneously. A delay associated with a multiplication string is the time that signals spread across the gate that form a multiplication string. Multiple multiplication is another important multiplication algorithm. For the multiplication of high-speed and exponential operations, large sets of stands are required which require large partial quantities and partial registers. The expansion of two n-bit operands using a radix-4 multiplier to record the cabin requires an estimated n / 2m cycle cycle to generate less than half of the final product, where m is the number in the stages of adding the recorders to the booths. Therefore, a large expense expense is associated with this case. Due to the importance of DSP digital multipliers, it is always an active research place and a large number interesting multiplication algorithms are shown in the literature [4].

In this, Urdhva tiryakbhyam Sutra is applied for the first time to a binary numbering system and is used to develop a digital multiplication architecture. It turned out to be very similar to popular multiplier architecture. This Sutra also shows the efficiency of reducing the NXN multiplication structure in an efficient 4X4 multiplication structure. It is considered that Nikhilam Sutra is more effective in multiplying large quantities by reducing the multiplication of two large numbers to two smaller ones. The proposed multiplication algorithm is illustrated to show its computational efficiency, giving an example of reducing the multiplication of 4X4 bits to a 2X2 binary multiplication operation [4]. This article presents a systematic design methodology for a fast and efficient multiplier based on vedic mathematics.

II. VEDIC MATHEMATICS

Vedic mathematics is part of the four Vedas (books of wisdom). About the Sthapatya-Veda (Book of Civil Engineering and Architecture), which is a UPA-Veda (surcharge) from the Atharva Veda. Provide information on different mathematical terms, including arithmetic, geometry (plan, coordinate), trigonometry, quadratic balances, and even math.

His army Jagadguru Shankaracharya Bharati Krishna Maharaja Teerthaji (1884-1960) understood all this work, and gave his mathematical explanation while eliminating several applications. Swamiji is composed of 16 sutras (formula) and 16 UPA sutras (sub formulas) after extensive research on Atharva Veda. Obviously, these formulas can not be seen in the current text of the Atharva Veda because these formulas were built in Swamiji itself. Vedic mathematics is not just an amazing math but also a logical one. So it has a kind of noble nature that can not be denied. Due to these remarkable traits, Vedic mathematics has already crossed the boundaries of India and has become an interesting topic of international research. Vedic mathematics deals with some basic and complex mathematical operations. Especially, the basics of arithmetic methods are the most simple and powerful [2,3].

The word "Vedic" is derived from the word "Veda" which means selling all knowledge. Vedic mathematics is based on 16 sutras (aphorisms) that speak of various mathematical branches such as arithmetic, algebra, geometry, and so on. [15]. These Sutras, with their shortest possible meanings, are listed under the alphabetical order.

1.(Anurupye) Shunyamanyat – If one is in ratio, the other is zero.

2. Chalana-Kalanabyham – Differences and Similarities.

3. Ekadhikina Purvena – By one more than the previous One.

4. Ekanyunena Purvena – By one less than the previous one.

5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.

6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.

7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.

8. Paraavartya Yojayet – Transpose and adjust.

9. Puranapuranabyham – By the completion or noncompletion.

10. Sankalana- vyavakalanabhyam – By addition and by subtraction.

11. Shesanyankena Charamena – The remainders by the last digit.

12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.

13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.

14. Urdhva-tiryagbhyam – Vertically and crosswise.

15. Vyashtisamanstih – Part and Whole.

16. Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be used directly in trigonometry, simple and open geometry, conical, calculations (both the same and integral), and the use of maths in different types. As mentioned above, all these sutras are reconstructed from the ancient Vedic writings of the last century. Many sub-sutras are also discovered at the same time, not mentioned here. The beauty of Vedic mathematics lies in the fact that it improves the calculation of several mathematical mathematics in a very simple way.

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This is because Vedic formulas are based on natural principles used by human thought. It is a very interesting field and it has some effective algorithms that can be used in several branches of engineering, such as computer science and digital signal processing [1.4].

Multiplier architecture can be classified into three categories. The first serial multiplier emphasizes that the hardware. And the minimum amount of chip area. The second is parallel multiplier (matrices and trees) that manages high-speed mathematical operations. But the disadvantage is that the cost of larger chip zones is relatively low. The third is a serial-parallel multiplier that acts as a good compensation among the areas used by serial multiplier and parallel multiplier.

III. DESIGN OF VEDIC MULTIPLIER

A.Urdhva Triyagbhyam(Vertically and Crosswise)

Urlhva tiryakbhyam sutra is a general formula of multiplication applicable to all cases of multiplication. Literally means "vertically and transversally." To illustrate this multiplication scheme, consider the multiplication of two decimal numbers (5498 × 2314). Conventional methods will require 16 multiplications and 15 additions.

An alternative method of multiplication with the Urdhva tiryakbhyam Sutra is shown in Fig. 1. The multiplied number is written on two contiguous sides of the zoo as shown in the figure. The square is divided into columns and columns where each row / column is equal to one digit to a multiplier or multiplier. Therefore, each digit of the multiplier has a small box normally a single digit when multiplied. These small boxes are divided into two halves by lines. Each digit of the multiplier multiplies each digit in multiple and the two-digit product is written in a common box. All the numbers located in a saved point are added to the front door. The most important number of digits of the acquired data is the resulting digit and the other as the next step. Bringing the first step (that is, the dotted line on the right side) was taken zero [9].

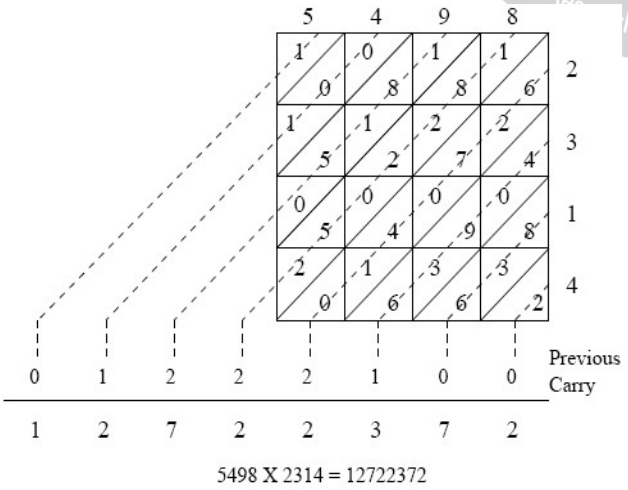

Figure 1: Alternative way of multiplication by Urdhva tiryakbhyam Sutra.

The design begins with the design of Multiplier, a 2x2-bit multiplier as shown in Figure 2. Here, the "Urdhva Tiryakbhyam Sutra" or "Vertical and Transverse Algorithm" [4] for multiplication is used to actually develop the digital multiplier architecture. This algorithm is different from the traditional method of adding, consisting of adding and replacing partial products.

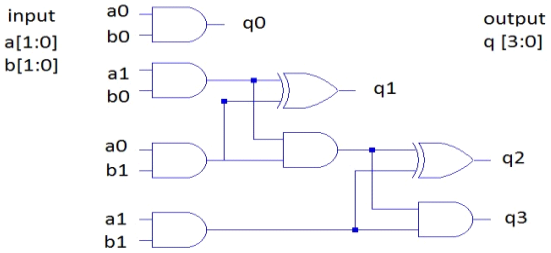

Figure 2: Hardware Realization of 2x2 block

To better understand the multiplier, the Karatsuba-Ofman algorithm can be used [6]. The Karatsuba-Ofman algorithm is considered one of the easiest ways to increase the number of integers. It is based on the fun and remission strategy [11]. The increase in the whole number of 2 digits is reduced to the multiplication of two digits, one (n + 1) digit number, another two digits, two operations without action, two additions and two have an increase of 2 digits.

The algorithm can be described as follows:

Make X and Y the binary representation of two integers:

$$X = \sum_{i=0}^{k-1} x_i 2^i$$

$$Y = \sum_{i=0}^{k-1} y_i 2^i$$

We want to introduce the product XY. Using the diversion and resistance strategy, X and Y operations may decay into the same size XH and XL, YH and YL, where the subscripts H and L represent high and low particle X and Y.Let k= 2n. If k is odd, it can be right padded with a zero

$$X = 2^n \sum_{i=0}^{n-1} x_{i+n} 2^i + \sum_{i=0}^{n-1} x_i 2^i = X_H 2^n + X_L$$

$$Y = 2^n \sum_{i=0}^{n-1} y_{i+n} 2^i + \sum_{i=0}^{n-1} y_i 2^i = Y_H 2^n + Y_L$$

The product XY can be computed as follows:

$$P = X * Y$$
$$= (X_H 2^n + X_L)(Y_H 2^n + Y_L)$$
$$= 2^{2n}(X_H * Y_H) + 2^n((X_H * Y_L) + (X_L * Y_H)) + (X_L * Y_L)$$

For the multiplier, the first blocks are the first, the 2x2 bits multiplier made, and then the blocks with the 4x4 block is done by adding partial products using the operator instead of the adders and then using this block 4x4, block of 8x8 bits, 16x16 bit block and a 32x32 bit multiplier as shown in Figure 3 made [7].

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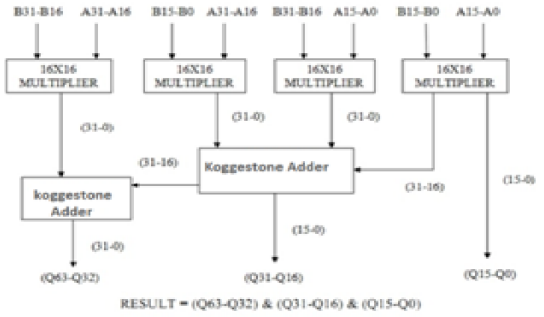

Figure : 32X32 Bits proposed Vedic Multiplier

Figure 3: 32X32 Bits proposed Vedic Multiplier

IV. IMPLEMENTATION OF VEDIC MULTIPLIER

Proposed multiplication is implemented using two different coding techniques, such as parallel prefix additives and Vedic techniques for 32 bit multiplier. Clearly, there is a great increase in the enthusiasm of Vedic architecture. The results of the multiplier works of 32 bit is shown in Figures 4. (a), each.

Simultion Results

Figure 4(a): 32 Bit Vedic Multiplier

Synthesis Results
SelectedDevice: xc3s1000l-4ft256
Number of Slices: 1440 out of 7680 18% Number of 4 input LUTs: 2534 out of 15360 16%
Number used as logic: 2534
Number of IOs: 128
Number of bonded IOBs: 128 out of 173 73%

S.No.	Parameters	Existing	Available	Proposed	Increase/Decrease
1.	No. of Slices	1947	7680	1440	26.04% decrease
2.	No. of 4input LUT's	3431	15360	2534	26.2% decrease
3.	No. of Bonded IOB's	128	-	128	No change
4.	Time Delay	111.127ns	-	121.214ns	1% increase
5.	Power	97.34	-	97.34	No change

Table 1: Delay composition for existing multipliers

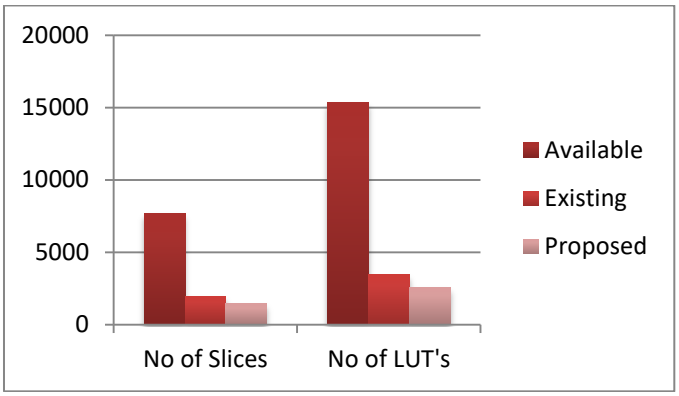

Fig 5:comparison of existing and proposed

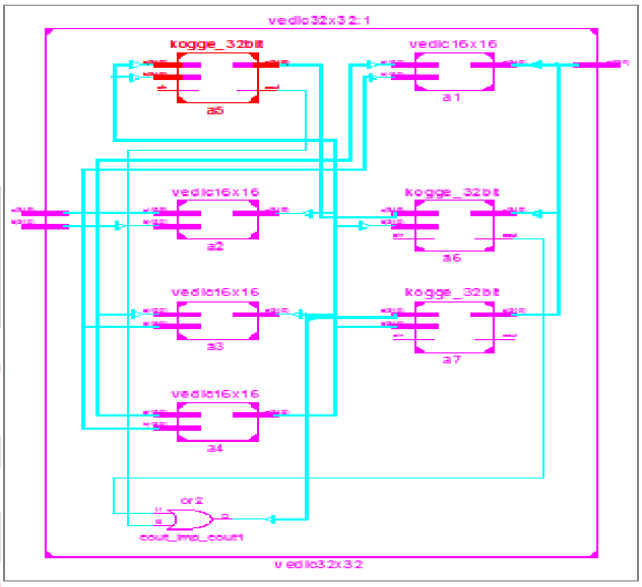

Fig 6:RTL schematic

V. CONCLUSION

The 32x32 bits Vedic multiplier designs have been implemented in Spartan XC3S1000l-4ft256. The existing area has taken more area compared to our proposed work. The proposal has taken a global area that has dropped by around 26%. Therefore, this architecture is comparatively better with respect to the previous architecture. Although the delay is different in both the architectures and the proposed work, the area lag product is less.

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