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Design of New Four Bit Reversible Array Multiplier Architecture and Its Performance Comparison

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Abstract - Reversible logic circuits are the circuits having same number of inputs and outputs, and have one-to-one mapping between vectors of inputs and outputs. Consequently, a computation is reversible, if it is always possible to recover the input for the given output. Multipliers play a vital role in today's digital signal processing and various other applications.It is an important hardware unit which decides the speed in any processor. The existing array multiplier is designed using Feynman, Toffoli and New reversible gates. In the existing array multiplier architecture the power consumption is high and the performance is low. In order to overcome these disadvantages, this work presents a reversible synthesis of array multipliers implemented with reversible k-CNOT gates(CC,CASS and CTRL). This work has been simulated using the xilinx simulator and verilog code, its parameters are compared with existing reversible array multipliers.

Keywords: reversible, feynman, new, tofolli, cass, cc, ctrl, xilinx

I. INTRODUCTION

In digital circuit design and synthesis, reduction of energy is the major goal. As reported by Landauer [1], usage of traditional (irreversible) logic gates leads to information loss and results in inherent energy loss in a circuit, disregarding its realization. A reversible system is always information lossless. Bennett [2] presented how zero-energy dissipation would be possible only in the case when the network consists of reversible gates. Over the past decade, many gates of reversible logic have been proposed like the controlled-not (CNOT) by Feynman [3], Toffoli [4], and Fredkin [5] gates. A reversible circuit consisting of reversible gates should be devoid of any fanout and feedback. This work proposes a reversible synthesis of the array multipliers. The proposed circuit has the ability to multiply (n x n) - bit binary numbers. It has been shown that the proposed design technique generates the reversible array multiplier circuit with least number of gates as well as least number of garbage outputs in comparison to earlier designs [6]–[8].

II. PRELIMINARIES

A. Reversible circuit:

A reversible circuit is a circuit with the same number of inputs and outputs and maps a input vector to a single output vector and vice versa. The following are the different reversible gates. 1) 1-input/1-output NOT (x1 → x1); 2) 2-input/2-output controlled NOT (CNOT) gate: (x1,x2) → (x1,x1 ⊕x2); and 3) 3-input/3-output Toffoli gate (x1,x2,x3) → (x1,x2,x1x2 ⊕x3).

Fig. 1. Reversible NOT

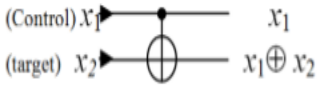

Fig. 2. CNOT Gate

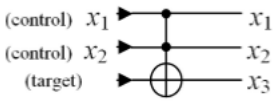

Fig. 3. Toffoli Gate

B. Toffoli gate:

A generalized Toffoli gate has a set of control inputs (C), a target input set(T), and has the form TOF(C:T), where C = (xi1,xi2,,xik), T = {xj} and C ∩ T = Ø. It maps the input vector (x0 1,x0 2,,x0 n) to the vector (x0 1,x0 2,,x0 j−1,x0 j ⊕ (x0 i1.x0 i2..x0 ik),x0 j+1,,x0 n). Thus, a NOT gate is (TOF(xj)), a generalized Toffoli gate which has no control inputs. The CNOT gate is (TOF(xi : xj)), a generalized Toffoli gate with one control bit is known as the Feynman gate. The simple (3- input|3- output) Toffoli gate

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is a generalized gate with two control inputs. The Toffoli gate with control inputs is shown in Fig. 3. A k-CNOT gate has k control inputs x1, x2,…., xk and one target input t. It maps the input vector (x1,x2,…,xk,t) to the output vector (x1,x2,….,xk ⊕x1.x2xk). In other words, a k-CNOT gate has (k +1) inputs and (k +1) outputs; the first k outputs follows the respective inputs and it negates the target at the (k+1)th output if and only if all the k control inputs are equal to 1. Any reversible function can be realized as cascading of k-CNOT gates.

C. Garbage outputs:

The garbage outputs are required to realise the given function and to ensure reversibility.

III. REVERSIBLE SYNTHESIS OF ARRAY MULTIPLIER

In this section, we propose the reversible synthesis of the array multiplier.

To design the reversible array multiplier, we need to design the reversible CASS cell circuit and reversible CTRL circuit using only k-CNOT gates. In CASS circuit, the expressions for the output functions are given in eqns. 1 and 2. From the expression of the Pout output function in eqn 1, we can easily map it in the reversible domain. Our aim is to express the Cout output function as a sum of exclusive-or functions. The sum-of-products (SOP) expression for the output function Cout in eqn 2 depending on the values of H and D is given in the table I. To achieve reversible synthesis of Cout we derive the Sum-of EXOR expression for Cout. a) : First, we express the sum-of-EXOR expression for the expression (a.b + b.c + c.a). It can be proved that a.b + b.c + c.a = a.b⊕b.c⊕c.a (3) Using the above identity, we can write the above output functions as follows:

When D = 0,

Cout = Pin.a + Pin.Cin + a.Cin
= Pin.a⊕Pin.Cin ⊕a.Cin

When D = 1,

Cout = Pin.a + PinCin + a.Cin
= Pin.a⊕Pin.Cin ⊕a.Cin

In general,

Cout = (Pin ⊕D).a⊕(Pin ⊕D).Cin ⊕a.Cin
= (Pin ⊕D).(a⊕Cin)⊕a.Cin

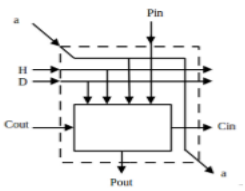

Fig. 5. CASS Cell

To achieve the reversible synthesis of the CASS cell circuit, we need only one constant input 0 and one extra garbage output. The block diagram of reversible CASS cell and the reversible circuit for this CASS cell using only k-CNOT gates are shown in Figs. 6 and 7 respectively. We have added one constant input (0) line and one extra garbage to obtain the reversible synthesis CTRL cell. The inputs and outputs of CTRL circuit are {xi,xi−1} and {H,D} where H = xi ⊕xi−1 and D = xi.xi−1.

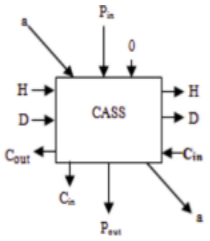

Fig.6.Block diagram of reversible CASS Cell

The block diagram and its reversible implementation of CTRL cell circuit are shown in the Fig. 8 and Fig. 9 respectively. Now we can write H = xi ⊕ xi−1 and D = xi ⊕xi.xi−1

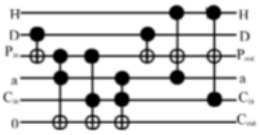

Fig.7. Block diagram of Reversible CASS cell using k-CNOT gates

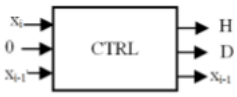

Fig. 8. Block diagram of CTRL Circuit

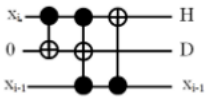

Fig. 9. Reversible CTRL Circuit

It is well known that there is no concept of fan-out in reversible circuit. We have used copy circuit as shown in Figs. 10 and 11 to avoid fan-out problem in reversible circuit.

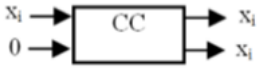

Fig. 10. Block diagram of COPY Circuit

Fig. 11. Reversible COPY Circuit

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Using three reversible cells CASS, CTRL and CC, we have constructed the reversible Array Multiplier as shown in the Fig. 12.

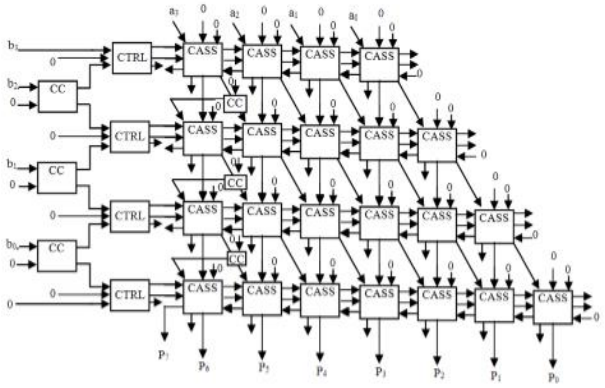

Fig. 12. 4x4 Reversible array multiplier

IV. PERFORMANCE EVALUATION OF THE PROPOSED REVERSIBLE ARRAY MULTIPLIER

Our proposed reversible array multiplier circuit is more efficient than the existing circuits presented in [6]–[8] in terms of garbage outputs and number of gates. We have presented the comparisons with different techniques in Table 1.

TABLE 1 COMPARATIVE EXPERIMENTAL RESULTS OF DIFFERENT 4X4 MULTIPLIER CIRCUITS

Circuit	No. of gates	No. of garbage outputs	Total logical calculation
Our proposed Circuit	22 CASS + 4 CTRL = 26	37	$128a + 70\beta$
Existing Circuit [6]	16 PG + 12 MKG = 28	56	$92a + 52\beta + 36d$
Existing Circuit [7]	16 FRG + 12 NG + 12 TG = 40	56 +68d	$80a + 100\beta$
Existing Circuit [8]	16 FRG +13 TSG=29	58	$110a + 103\beta + 71d$

Quantum simulation has been done for the array multipler using the Xilinx simulator [8]. The highlighted

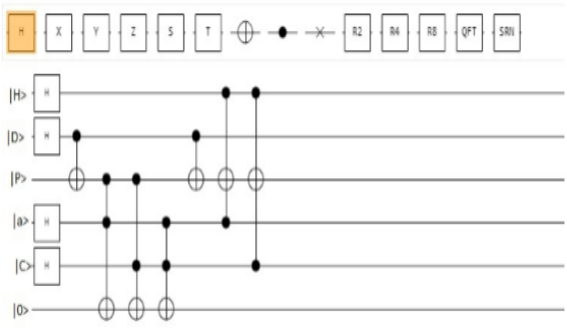

Fig. 13. Simulation when Pin = 0 and Pin = 1

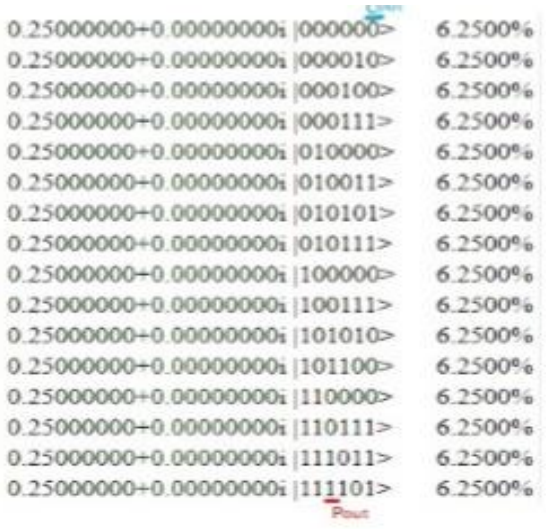

Fig. 14. Table for simulation when Pin is 0

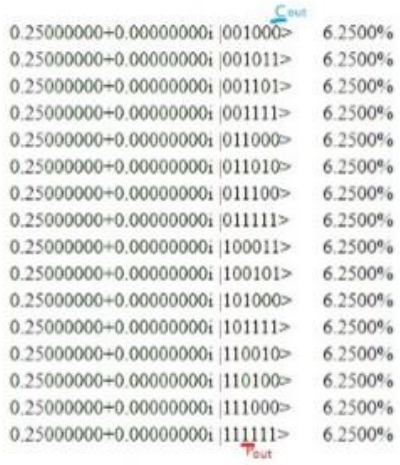

Fig. 15. Table for simulation when Pin is 1

operations in Fig. 13 has been simulated and the simulation results as obtained by the Xilinx simulator [8], are presented in Figs. 14 and 15. a) : We have compared our proposed circuit with the existing circuits in [6]–[8] and it is found that our proposed design approach requires 26 gates if we do not count the CC (reversible copy gate) gates. In the table, the used terms represents as follows:

a = A two input EX-OR gate calculation β = A two input AND gate calculation d = A NOT calculation T = Total logical calculations

b) : Garbage output refers to the output of the reversible gate unused as a primary output or as input to other gates. One of the major constraints in synthesis of a reversible logic circuit is to have lesser number of garbage outputs. Our proposed reversible array multiplier circuit produces 37 garbage outputs which are very less compared to the results of [6]–[8]. From the above discussion, we can conclude that the proposed reversible array multiplier circuit is better in performance than the existing array multiplier.

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V. SIMULATION RESULTS

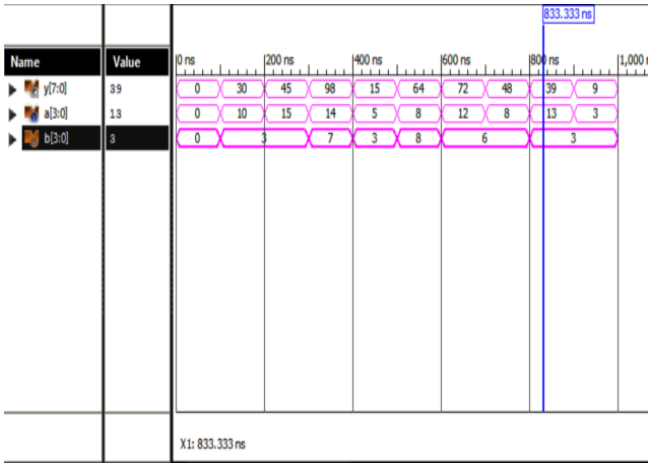

Fig. 16 Simulation result

The above figure is the simulation result of the proposed reversible array multiplier. It is simulated using Xilinx simulator. In the above figure a & b are the four bit inputs and y is the output. Here we can see a number of combinations of inputs and the resultant output. For example when a=10 , b=3 then the result y=30.

VI. RTL SCHEMATIC

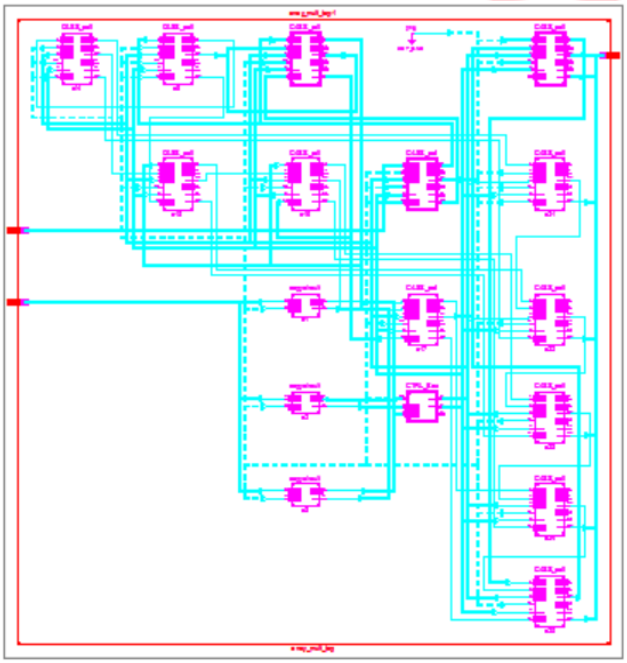

Fig: RTL Schematic

The above figure shows the RTL(Register Transfer Level) schematic of the proposed reversible array multiplier. This is generated from the Xilinx simulator.

VII. RESULTS COMPARISION

Parameter	Existing model	Proposed model
No of unused outputs	56	37
No of zero inputs	32	46
Power consumption	80.38mW	57.58mW
Time delay	15.934ns	17.598ns
No of slice LUTs	18	27
No of fully used LUT-FF pairs	0	0
No of bonded IOBs	16	16

Fig: comparision between existing and proposed model

Power is one of the most important criteria for designing any system. As the functionality of the system increases, power consumption of the system also increases. Hence reducing the power consumption of the system is of utmost priority. The above comparision table shows the differences in values for various parameters of existing and proposed models. From the table we can see that the power is reduced in proposed model.

VIII. CONCLUSION

This work proposes a reversible synthesis of the array multipliers implemented with reversible k-CNOT gates which are delay efficient when compared to the existing reversible array multiplier. The proposed design technique generates a reversible array multiplier circuit with least number of gates as well as least number of garbage outputs as compared with existing techniques. The operations of the array multiplier have been verified using standard Xilinx simulator .

Reversible logic gates can be used to reduce the power consumption of the circuits. Therefore the basic gates can be replaced by reversible logic gates to achieve the power minimisation.

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