High Speed and Area Efficient Accuracy Configurable Adder

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Abstract: In the field of VLSI to attain optimizing speed and power consumption becomes a challenging task in the design of any reliable and efficient Integrated Circuit (IC). To overcome this, a few Accuracy Configurable Adder (ACA) design are developed. In the existing design, it occupies large area for the carry prediction technique to attain accurate result. In the present work, it uses Carry Select Adder (CSLA) and modified Half Sum Carry Generation (HSCG) based Square Root (SQRT)-CSLA are preferred as baseline adder of ACA. Among these baseline adders, the modified Half Sum Carry Generation (HSCG) based Square Root (SQRT) -CSLA is found to be more efficient than the normal CSLA. The proposed ACA in carry prediction technique attain less latency. Hence, the proposed design is proved to be more efficient than existing designs such as RCA with carry prediction technique. The simulation designs are carried out by using software prototype tool of Quartus II-8.1v. Thus the proposed design shows the efficiency in-terms of tradeoff between delay, area and power.

Keywords — Approximate Computing, Accuracy Configurable Adder (ACA), delay, Half- Adder Sum Carry Generation (HSCG) based SQRT-CSLA.

I. INTRODUCTION

In recent years, Low power, area efficient and high performance VLSI system designs play an important role in advanced digital processors. Adders are the key component in general purpose microprocessors and digital signal processors. Adders are not essential only for addition, but also it is worth full for subtraction, multiplication and division. For high performance processors and systems high-speed addition and multiplication have always been a fundamental requirement. In the field of digital circuit the delay increases during carry propagation. To overcome such delay the conventional adder of CSLA is used in many computational systems in order to reduce the propagation delay. There are many types of adder designs available, each of them have own advantages and disadvantages. The Modified structure of Half Adder Sum Carry Generation (HSCG) based Square Root Carry Select Adder (SQRT-CSLA) is constructed to reduce the number of gates required.

II. LITERATURE SURVEY

In In the last 20 years, a lot of research was done to improve the speed and power consumption. Half-adder Sum Carry Generation (HSCG) Unit based Square Root (SQRT-CSLA) is the adder that occupies the less area compared to the conventional CSLA.

Numerous designs were realized for the ACA functions using different number of design techniques and approaches [1], [2], [3], [4], [5], [6], [7], [8], [9], [10] and [11]. Each design differs from one another. The early design of accuracy adder depends on the ACA techniques. Baseline adder of RCA is used in **[1]**. It is same as that of the conventional adder, but for the carry propagation it uses the carry prediction technique to attain accurate result with less latency. Omid Akbari **[2]** proposed another accuracy adder based on the carry look a-head adder it operates on both accurate and inaccurate mode. It has the disadvantages of more area and power consumption while compared **[1].** Square root carry select adder is proposed in **[3].** This technique is modified of the conventional CSLA. It overcome the problem occurred in CSLA because it consists of multiple RCA and multiplier for Sum, Carry generation. The proposed adder consumes less area and delay for carry propagation. In **[4], [5]** and **[6]** proposed an efficient design of CSLA. The difference is that it uses the BEC-1 and SCG (Sum Carry Generation) unit instead of RCA for the CIN ='1'. In the **[8]** and **[9]** the proposed design has less delay, area and reduced the redundant logic.

Muhammad Shafique **[7]** proposed an ACA with less delay under the approximate mode. For the error correction it integrated the external circuit to attain the accurate result. It is implemented in Xilinx virtex-6 FPGA. It has more area utilization while compared to **[1].** In **[10]** proposed an approximate arithmetic design based on ACA. It operates on both accurate mode and inaccurate mode based on the application uses. For this arithmetic design it uses EDC

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technique of ACA method. While compared to the conventional adder it decreases the total power consumption to attain accurate result under the dynamic mode.

III. METHODOLOGY FOR THE PROPOSED ACA

This section describes about the steps which are involves for the design of proposed ACA.

- Choosing the adder from the conventional technique.
- Here in this proposed, CSLA and HSCG based SQRT-CSLA selected from the conventional list.
- Implement the adder in prototype tool, the adder which is taken from the conventional adder method.
- To attain the accurate result of sum and carry for this adder.
- After getting the accurate result, the elected adder is design by using ACA technique.
- The ACA technique used here to get accurate and approximate carry.
- The accurate carry is the total carry of the adder, but the approximate carry is the half the portion of the carry.
- Based on the application the carry is generated, but the both carry attains accurate result.

IV. PROPOSED DESIGN OF ACA

Accuracy Configurable Adder (ACA) is used to configurable the accuracy of results during run time it holds a great promise for low power IC design in the field of advance VLSI technologies. Because of its configurability, the ACA adder can adaptively operate in both inaccurate (approximate) mode and accurate mode. Both modes of operation give accurate result. Instead of using the accurate mode it is better to use inaccurate mode to attain accurate result.

By using this approximate mode, it attains efficiency in-terms of power, delay and area (number of logic gates). With the help of conventional Carry Select Adder (CSLA) and modified HSCG based SQRT-CSLA methods a new ACA is designed based on the carry prediction technique in order to reduce the latency during the carry propagation.

4.1 Accuracy Configurable Adder Based on CSLA

A new carry prediction based Accuracy Configurable Adder (ACA) is proposed. While compared to the existing method it has the following advantages: no error correction or detection circuit, no redundancy, no data stall, latency is less and it attains the better accuracy. The proposed ACA is used for the application of image processing and so on. The proposed adder is configured by the mode of carry prediction. It operates on both accurate and approximate condition. Operating in approximate condition attains the accurate results and the delay is also reduced compared to the accurate condition.

A. Working of CSLA based ACA

The proposed 8-bit ACA consists of sub adder, carry in and carry out blocks. Except the carry in and carry out every block is same as that of the conventional Carry Select Adder (CSLA). In this method, 8-bit adder is composed of K segment of L-bit sub adders (i.e. K = [N/L]). It uses the same sub adder block for carry prediction without adding additional unit. The block diagram of 8-bit CSLA based on ACA is shown in Fig. 1.

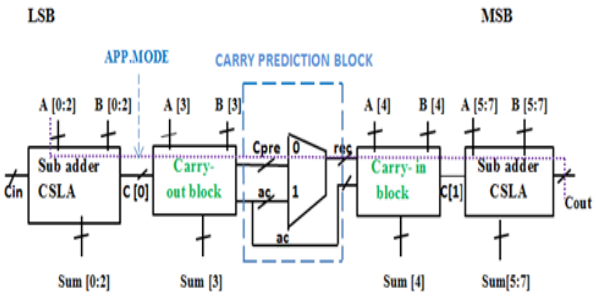

Fig. 1: 8-bit CSLA based on ACA

It is useful for the high speed circuit. In this proposed method 8-bit ACA is developed on the conventional adder of CSLA. CSLA operates in both condition of CIN = '0' and '1' parallel and the required part get through the multiplexer operations. Each sub adder is almost same as CSLA except that the MSB of a sub adder, which is bit i, provides a carry prediction by $C_i^{prdt} = gi$. The logic diagram of proposed CSLA based on ACA is shown in Fig. 2.

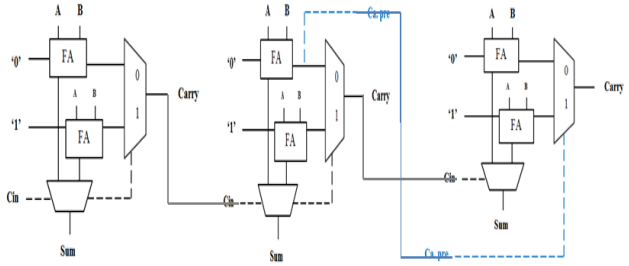

Fig. 2: Logic diagram of proposed CSLA based on ACA

It consists of three blocks:

- Sub adder of CSLA
- Carry out block of CSLA
- Carry in block of CSLA

B. Sub adder block of CSLA

Carry Select is one of the fastest adders. The structure of 3-bit CSLA is shown in Fig. 3. It consist of RCA with the four multiplexer to select SUM and CARRY from input of CIN ='0' and CIN ='1' through the multiplexer input of

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CIN. The truth table of 3-bit CSLA is shown in Table 1. The upper adder has a carry in of zero, the lower adder a carry-in of one.

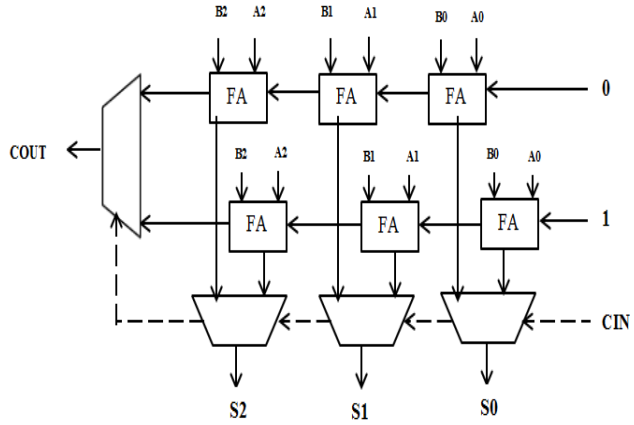

Fig. 3: Block diagram of 3-bit CSLA

The actual CIN from the preceding sector selects one of the two adders. The conventional Carry select adder is efficient than the Ripple carry Adder (RCA).

Table 1: Truth table of 3-bit CSLA

	INPUT							OUTPUT			
	CIN	A2	A1	A0	B2	B1	B0	S2	S1	S0	COUT
When CIN ='0'	0	0	0	1	1	0	0	1	0	1	0
	0	0	0	0	1	1	0	1	1	0	0
	0	1	1	1	0	0	1	0	0	0	1
	1	1	0	0	0	1	0	1	1	1	0
	1	0	1	0	1	0	1	0	0	0	1
	1	0	1	0	1	1	0	0	0	1	1

C. *Carry out block of CSLA*

A carry out block of configurable CSLA consists of A, B and CIN as input and output as SUM, CARRY and CA. PRE. In Fig. 4, when CIN = '0' it computes sum and carry for the input of '0' and vice versa for CIN = '1'.

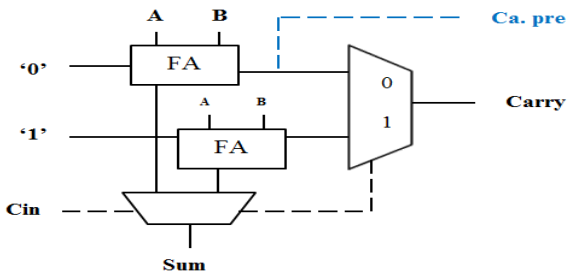

Fig. 4: Carry out block of CSLA

In carry out block of configurable CSLA consists of two full adders and two multiplexer. It computes sum and carry for the input of A, B and CIN. The operation of carry out block of configurable CSLA is performed based on CIN = '0' or '1' for the required input of full adder '0' and '1'. A Carry out block of configurable CSLA consists of two full adders and two multiplexer to generate Sum and Carry. The truth table for carry out block of configurable CSLA is shown in Table 2.

Table 2: Truth table of 3-bit CSLA

	INPUT							OUTPUT				
	CIN	A2	A1	A0	B2	B1	B0	S2	S1	S0	COUT	CAPRE
When CIN ='0'	0	0	0	1	1	0	0	1	0	1	0	0
	0	0	0	0	1	1	0	1	1	0	0	0
	0	1	1	1	0	0	1	0	0	0	1	1
	1	1	0	0	0	1	0	1	1	1	0	-
	1	0	1	0	1	0	1	0	0	0	1	-
	1	0	1	0	1	1	0	0	0	1	1	-

D. *Carry in block of CSLA*

For the LSB of the higher bit sub adder, which is bit i + 1, its carry out C_{i+1} can be computed by using one of two options, either by the conventional method $C_{i+1} = g_{i+1} + p_{i+1} * C_i$ or by using the carry prediction as $C_{i+1} = g_{i+1} + p_{i+1} * C_i^{prdt}$. In carry in block of configurable CSLA it consists of two full adders and two multiplexer. It computes sum and carry for the input of A, B and CIN. The carry in block of CSLA is shown in Fig. 5. The operation of carry out block of configurable CSLA is performed based on CIN = '0' or '1' for the required input of full adder '0' and '1'. It has extra input of carry prediction to compute accurate carry.

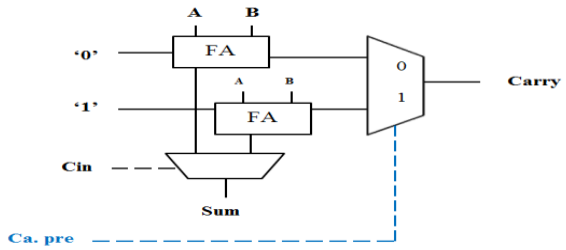

Fig. 5: Carry in block of CSLA

E. *Carry Prediction Block for CSLA*

Carry prediction block of CSLA is consists of sub adder, carry out block, multiplexer for carry prediction and carry in block. The prediction scheme makes a very simple modification to the conventional Carry Select Adder. Predicting carry must able to attain the accurate result with less latency, it is one of the major factors of Accuracy Configurable Adder. Approximate carry gained from the first set of full adder for the input of '0' it comes by forcing method (i.e. forcing input). Computation is same as for the conventional adders but delay is reduced.

For the multi bit adder the delay is depends on the propagation path. The logic diagram of carry prediction block of CSLA is shown in Fig. 6. This large delay reduction can be translated as the power reduction by supply voltage scaling. So intention is to only attain the higher accuracy.

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Table 3: Truth table of HSCG based SQRT-CSLA

INPUT			OUTPUT		
CIN	A	B	SUM	CARRY	CPRE
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

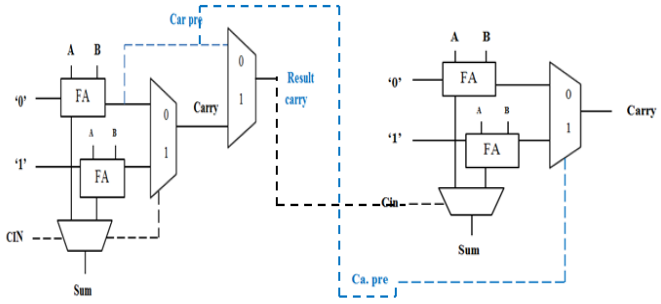

Fig. 6: Carry prediction block for CSLA

4.2 Accuracy Configurable Adder of HSCG based SQRT-CSLA

In this proposed method 8-bit ACA is developed for the half adder Sum Carry Generation (HSCG) based Square Root (SQRT) CSLA. Compared to the conventional CSLA this modified CSLA requires less number of gates. It consists of half adder, OR gate and two multiplexers, a HSCG unit and a SCG unit. Multiplexer is used to select the SUM and CARRY for the input of CIN = '0' or '1'. The block diagram of HSCG based SQRT-CSLA is shown in below Fig. 7. Each block is explained in below.

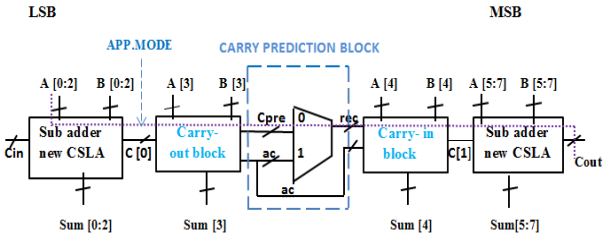

Fig. 7: Block diagram of HSCG based SQRT-CSLA

A. Half Sum Carry Generation (HSCG) BASED Square Root (SQRT) CSLA

A HSCG based SQRT-Carry Select Adder design have a (Half Sum Carry Generation) HSCG Unit and (Sum Carry Selection) SCS Unit. It reduces the number of logic gates compared to RCA and CSLA. The input CIN is selects the sum and carry using multiplexer. The block diagram and truth table of HSCG based SQRT-CSLA is shown in Fig. 8 and Table 3.

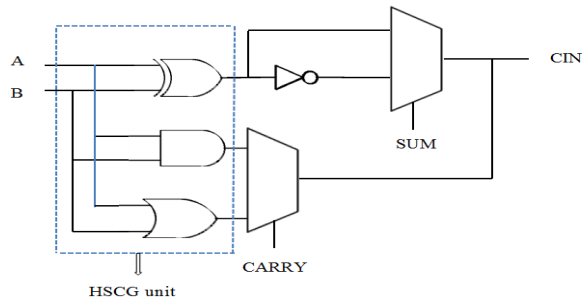

Fig. 8: Block diagram of HSCG based SQRT-CSLA

This Corresponding architecture gate count takes only four logic gates and two multiplexers. The CS unit selects one final carry word from the two carry words available at its input line using the control signal CIN.

When CIN = '0' the sum and carry is represented in Boolean equation is

$$SUM = A \text{ XOR } B \quad (1)$$
$$CARRY = A \text{ AND } B \quad (2)$$

While CIN = '1' the sum and carry generation is

$$SUM = \overline{A \text{ XOR } B} \quad (3)$$
$$CARRY = A \text{ OR } B \quad (4)$$

B. Carry out block of HSCG based SQRT-CSLA

Carry out block of HSCG based SQRT-CSLA is different from the normal HSCG SQRT CSLA. It is used to propagate two types of carry signal. They are accurate and approximate carry. With the grown technology, the size of transistor is getting reduced. For that purpose the approximate computing with accurate carry is used in many data processing applications. The logic diagram of carry out block of HSCG is shown in Fig. 9. The advantage of carry out block is that it predicts both actual carry and predicted carry.

When CIN = '0' the sum and carry is represented in Boolean equation is

$$SUM = A \text{ XOR } B \quad (5)$$
$$CARRY = A \text{ AND } B \quad (6)$$
$$CARPRE = A \text{ AND } B \quad (7)$$

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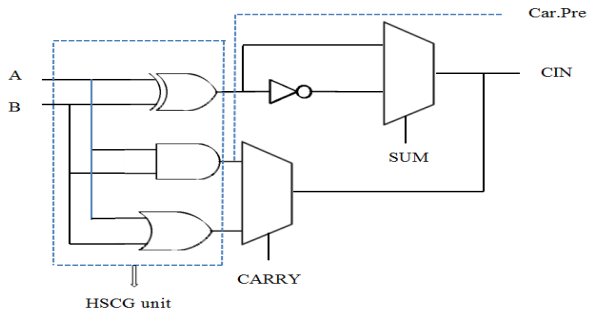

Fig. 9: Carry out block of proposed HSCG based SQRT-CSLA

While CIN = '1' the sum and carry generation is

$$SUM = \overline{A \text{ XOR } B} \quad (8)$$

$$CARRY = A \text{ OR } B \quad (9)$$

The truth table of carryout block of HSCG is shown in Table 4.

Table 4: Truth table of proposed carry-out HSCG based SQRT-CSLA

INPUT			OUTPUT		
CIN	A	B	SUM	CARRY	CPRE
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

C. Carry in block of HSCG based SQRT-CSLA

Carry in block of HSCG based SQRT-CSLA is configured by using one half adder block, two multiplexer for sum and carry generation, one NOT gate and one OR gate. The normal HSCG based SQRT-CSLA has two units, Sum and Carry generation (SCG) unit and Sum and carry Selection (SCS) units.

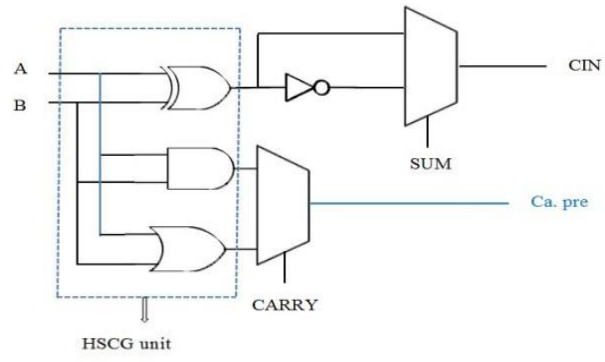

Fig. 10: Carry in block of proposed HSCG based SQRT-CSLA

The logic diagram and truth stable of Carry in block of proposed HSCG based CSLA is shown in Fig. 10 and Table 5.

When CIN = '0' and CPR = '0' then the sum and carry is represented in Boolean equation is

$$SUM = A \text{ XOR } B \quad (10)$$

$$CARRY = A \text{ AND } B \quad (11)$$

While CIN = '1' and CPR = '1' then the sum and carry generation is

$$SUM = \overline{A \text{ XOR } B} \quad (12)$$

$$CARRY = A \text{ OR } B \quad (13)$$

A separate input are used both SUM and CARRY generation they are CIN and CPRE.

Table 5: Truth table for carry in block of Proposed HSCG based SQRT-CSLA

INPUT				OUTPUT	
CIN	A	B	CPR	SUM	CARRY
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	1	1	1

V. RESULT ANALYSIS

This section demonstrates and analyses the results obtained from each of the circuits involved in developing the proposed Accuracy Configurable Adder (ACA).The major components of design of ACA are conventional Carry Select Adder (CSLA) and HSCG based SQRT-CSLA. The proposed design is verified by using Quartus II-8.1v. The entire design is coded by using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). The designs are followed by VLSI designs steps. At the last step of design it creates a file in .SOF format which is used for implement in ACEX1K hardware programmable devices. By using this prototype tools it helps to design and simulate an Analogue Integrated Circuits before going to the time consuming and costly process of fabrication of an IC. The simulation view of propose methods are shown in Fig. 11, 12.

5.1 Simulation Parameters

The parameters needed for the design of proposed ACA are

- Number of inputs : 17 (A, B, CIN)
  A= (A0, A1, A2, A3, A4, A5, A6, A7)

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B= (B0, B1, B2, B3, B4, B5, B6, B7)

- Number of outputs : 9 (SUM, COUT)
  SUM = (S0, S1, S2, S3, S4, S5, S6, S7)

- Number of bits to configured : 8

5.2 Simulation Result of ACA using CSLA

EXPRESSION:

SUM = A XOR B XOR CIN;

COUT = (A AND B) OR CIN (14)

INPUT:

A = 10010101; B = 01100010; CIN = 0

OUTPUT:

SUM = 11110111; COUT =0

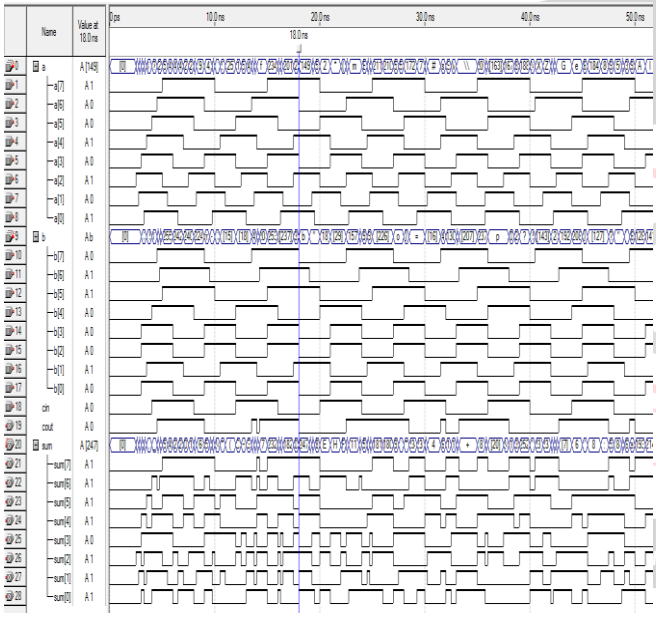

Fig. 11: Simulation view of carry in ACA using CSLA

5.3 Simulation Result of ACA using HSCG Based SQRT-CSLA

EXPRESSION:

SUM = A XOR B XOR CIN;

COUT = (A AND B) OR CIN (15)

INPUT:

A = 10111010; B = 10010001; CIN = 1

OUTPUT:

SUM = 11001100; COUT =1

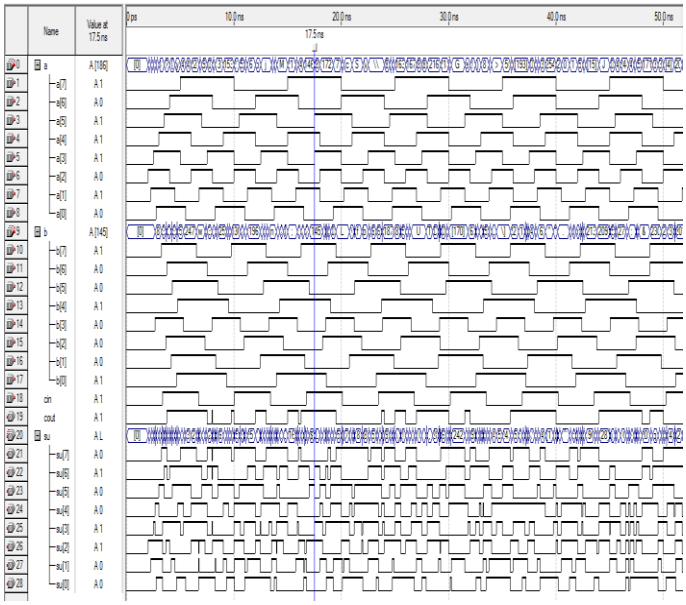

Fig. 12: Simulation result of ACA using HSCG based SQRT-CSLA

VI. COMPARISON

The comparison for various parameters like delay, area, total LE, number of I/O pins and ADDER are listed in the Table 5.1 Simulation results of ACA design are configured by using baseline adder of RCA, CSLA and modified HSCG based SQRT-CSLA. Among these modified HSCG based SQRT-CSLA shows less latency. Transistor count of RCA and HSCG based SQRT-CSLA for ACA is listed in Table 6. The propagation time is effective than the [1].

Table 6: Comparison of RCA, CSLA and HSCG based SQRT-CSLA

Sl. No.	PARAMETERS	EXISTING	PROPOSED	
1	ADDER	RCA	CSLA	HSCG based SQRT-CSLA
2	Total LE's	16	16	16
3	No. of I/O pins	26	26	26
4	Time delay for acc.carry (ns)	28.600	27.400	26.500
5	Time delay for appr.carry (ns)	24.500	23.500	21.300

VII. CONCLUSION

High speed Accuracy Configurable Adder (ACA) is designed by using the CSLA and modified HSCG based SQRT-CSLA with carry prediction techniques. The performance of proposed ACA's is simulated using Quartus II- 8.1v and implemented in Altera ACEX1K device. The

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proposed ACA's proves to be an easier solution for improving the speed of conventional adders. The conventional adders suffer from the disadvantage of occupying more chip area, which is overcome by carry prediction in ACA technique. The proposed ACA adder technique show less latency in comparison with conventional adders such as RCA, CLA and so on. The propagation delay of the proposed adder is obtained from the simulator tool used in Quartus II software. The proposed HSCG based SQRT-CSLA of ACA technique gives overall time delay of 21.300ns for approximate carry prediction and 26.500ns for accurate carry prediction. The proposed CSLA of ACA technique gives overall time delay of 23.500ns for approximate carry prediction and 27.400ns for accurate carry prediction.

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