Synchronizing Distributed Photovoltaic Generation with an Active Network (A review on Challenges and Different Schemes)

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Abstract: **Recent developments in photovoltaic technology offered end users to establish their own Distributed Photovoltaic plants and integrate them with the existing power network on commercial and beneficial basis. However, the high penetration of Distributed photovoltaic generation leads to poor power quality. With this issue, synchronization standards became substantially tough emerging new tedious rules of synchronization. Thus, giving distributed generation operators new deals to supply power with better standards, with better power quality. Which includes handling of Power Quality issues like Voltage rise effect, Reactive power Control, Harmonic compensation, Synchronization and Islanding. However, this paper focuses on Synchronization methods, comparison and Proposal of Suitable synchronization scheme.**

Keywords — DG: Distributed Generation, DGPV: Distributed Generation by Photovoltaic, PVI: Photovoltaic Inver, PCC: Point of Common Coupling, GSC: Grid side converter, DDSRF: Decoupled Double Synchronous Reference Frame, ETD: Enhanced Transfer Delay, SRF: Synchronous Reference Frame, PLL: Phase Locked Loop

I. INTRODUCTION

Since past few decades Distributed Generation (DG) played an important role in serving electricity to power network during peak and excessive loads. As DG units provides many potential benefits such as least running cost, free raw energy (solar, wind, geothermal etc.) and more importantly they are environmental friendly with comparable low cost [1,2]. Due to these advantages Distributed Generation has now become a wide era of interest to the Engineers. However, penetration of Distributed power with active network is not as easy as it looks. At the time of Synchronization, factors limiting the Integration of PV include the thermal rating of grid equipment, the rise in Voltage, Voltage fluctuations and reverse power flow [3].

II. DISTRIBUTED PHOTOVOLTAIC GENERATION

As illustrated in figure:1, structure of DGPV consists of multiple converters. These converters are classified into two main types called Input side converter and Output side converter [4]. The input side controller consists of MPPT to extract maximum power from PV array. Different Algorithms for MPPT are presented in [5] to optimize maximum power output with faster convergence speed along with better power quality. Each of the Algorithm can be applied to Grid connected and Stand-alone system with some modifications. An Input side controller also consists of a Booster to regulate DC voltage to be fed to PVI. Further, a grid side converter used in a DGPV can perform the following functions:

1. Control of active power to be injected
2. Control of reactive power transfer
3. Control of dc-link voltage
4. Ensure high quality of the injected power
5. Grid synchronization

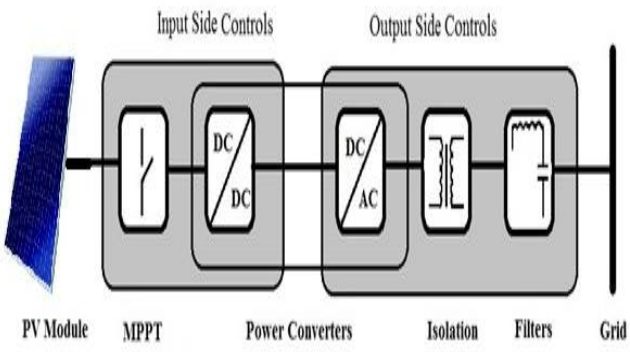

Fig:1. Structure of a DGPV

Apart from these, a Grid-side converter can be provided with some ancillary services like local voltage and frequency regulation, voltage harmonic compensation, or active filtering [4].

III. SYNCHRONIZATION

In terms of Distributed Generations, “Synchronization” is a process of connecting distributed sources into grid in parallel with many other alternators, that is in a live system

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of constant voltage and frequency. Equal Voltage, Matched frequency, Phase sequence and Voltage phase angle, these are the parameters which a synchronization scheme must satisfy before feeding power into the grid. A detailed Classification of Different Synchronization scheme is given in Fig: 2.

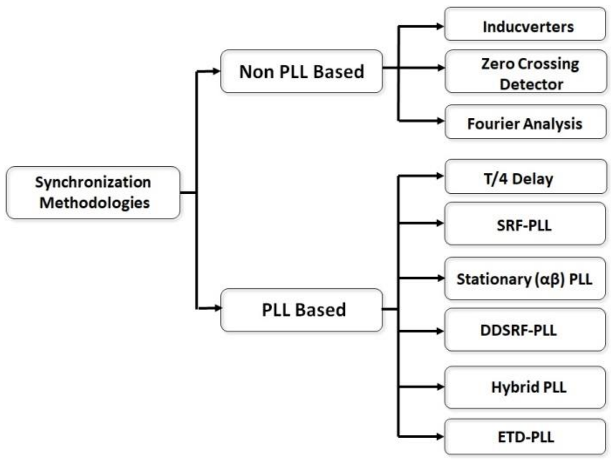

Fig: 2. Classification of Synchronization Methods

A DGPV synchronization system must be rugged, well designed and must be capable of dealing with technical problems. There are different synchronization schemes based on PLL and Non-PLL techniques. Non PLL based methods are Zero Crossing Detector (ZCD), Fourier analysis-based Synchronizer and Inducverters. However, ZCDs are more popular as it appears in simplest form and can be easily implemented [6]. In this technique zero-crossings are detected by capturing Rising and falling zeros of AC signal. To obtain the phase control, the phase difference between two input signals is extracted. But Zero Crossing Detection (ZCD) method fails when the synchronization signals contain multiple zero-crossings as in case of harmonics or noises. Another disadvantage of ZCD is that it has poor dynamic response due to one cycle or half cycle control [7]. To overcome these drawbacks, three-phase PLL based systems are implemented because they possess fast dynamic response, and accurate measurement of Phase angle and Frequency of Grid voltage and more reliable as compared with Non-PLL methods [8].

A. Phase Locked Loop

A phase-locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. PLL is a commonly used synchronization technique due to the advantages it offers such as simple in design and robust performance under ideal grid conditions [9]. For Grid synchronization a commonly used PLL is Synchronous Reference Frame (SRF) PLL. Basic scheme of which is as shown in Fig: 3.

It consists of three building blocks: a phase detector, a loop filter, and a voltage-controlled oscillator

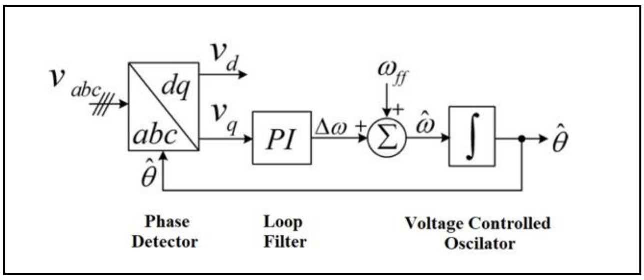

Fig: 3. Basic Scheme of Synchronous Reference Frame PLL

(VCO) [7]. A phase Detector compares the phase at each input and generates an error signal, $V_e(t)$, proportional to the phase difference between the two inputs. The Gain of Phase detector is K_D and it is Measured in V/rad.

$$V_e(t) = K_d\{\emptyset_{out}(t) - \emptyset_{in}(t)\} \ldots\ldots\ldots\ldots\ldots\ldots \text{(1)}$$

A "Low Pass Filter" is used in PLL to minimize the high frequency components in the output of the phase detector. It also removes the high frequency noise. Therefore, a Low Pass Filter (LPF) is an essential part in PLL and helps control the dynamic characteristics of the whole circuit. The dynamic characteristics include transient response of circuit, bandwidth and lock range. Lock range is a tracking range where the input frequency range is followed by range of frequencies of the PLL system. The capture range is the range in which the Phase Locked Loops attains the Phase Lock.

In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output.

$$\emptyset_{out} = K_{vco}\int_{-\infty}^{t} V_{cont}\, dt \ldots\ldots\ldots\ldots\ldots\ldots \text{(2)}$$

VCO oscillates at an angular frequency ω_{out} which is set to a Nominal Frequency ω_o when control voltage is zero. Frequency is assumed to be linearly proportional to the with a gain coefficient K_{vco} *Rad/s/v*.

$$\omega_{out} = \omega_o + K_{vco}V_{cont} \ldots\ldots\ldots\ldots\ldots\ldots \text{(3)}$$

According to the theory of SRF Voltage signals (abc variables) are transformed into d-q frame. And the transformation equation is

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 0 & -{}^{1}/_{2} & -{}^{1}/_{2} \\ 0 & {}^{\sqrt{3}}/_{2} & -{}^{\sqrt{3}}/_{2} \\ {}^{1}/_{2} & {}^{1}/_{\sqrt{2}} & {}^{1}/_{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \ldots\ldots\ldots \text{(4)}$$

The response of Stationary Reference Frame faces problems under unbalanced fault. This PLL Techniques fails to track phase angle under fault conditions.

Another type of PLL based on Enhanced Transfer Delay [ETD-PLL] uses small signal analysis to modify the transfer delay units required for the synchronization and to insert compensator gains in order to 'improve the overall PLL performance'. But it suffers from the drawback that Synchronization against low order harmonics may cause poor power quality of Grid Tied Inverter. Whereas a PLL

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based on Multi Harmonic Decoupling Cell [MHDC] possess the ability of Accurate Performance during Harmonic distortions with significantly less processing time. But again, it suffers from Increased implementation complexity [10].

A Hybrid PLL which is the combination of Stationary Reference Frame, SRF-PLL and Decoupled Double SRF, combines the advantages of all of the Three methods. As mentioned above an SRF-PLL is well suitable for balanced grid conditions. But under unbalance condition it fails to track accurately the phase angle.

B. Stationary Reference Frame PLL:

The Stationary Reference Frame (αβ-PLL) uses Clarke's Transformation to convert three phase AC variables into two phase orthogonal stationary system. The transformation equation is given by

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

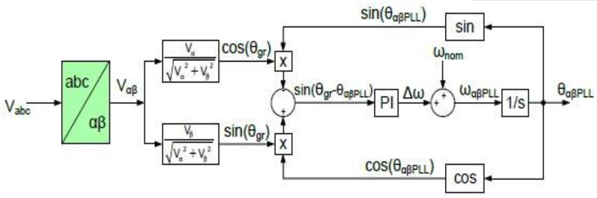

Fig: 4. Structure of Stationary Reference Frame

The objective of αβ-PLL is to induce the difference of phase angle between input and output signal. This deviation is to be controlled to zero by PI controller. But αβ-PLL again faces the same problem as SRF during Unbalanced condition [11].

C. Decoupled Double SRF-PLL:

A DDSRF consists of a decoupling network and phase locked loop operating SRFPLL. The decoupling network is used to provide positive sequence and negative sequence components from the input voltage vector. The positive sequence component of the grid voltage is synchronized when the positive sequence q-component is controlled to zero [12],[13].

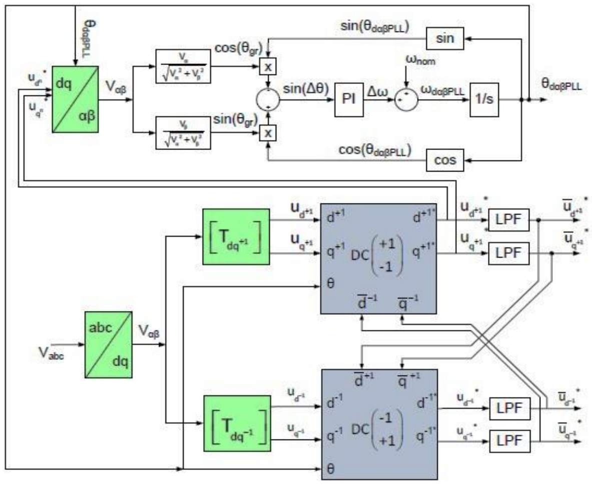

Fig:5. Structure of Decoupled Double SRF

As shown in fig:5, DDSRF has two SRFs. dq^{+1}, rotating with positive synchronous speed with angular position is +θ and dq^{-1}, rotating with negative synchronous speed with angular position is –θ. The voltage vector V, which consists of V^{+1} and V^{-1}, can be transformed into the dq^{+1} and dq^{-1} axes by Equation (6) and (7).

$$u_{dq^{+1}} = \begin{bmatrix} u_{d^{+1}} \\ u_{q^{+1}} \end{bmatrix} = [T_{dq^{+1}}]u_{ab} = V^{+1}\begin{bmatrix} 1 \\ 0 \end{bmatrix} + V^{-1}\begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} \ldots\ldots\ldots\ldots (6)$$

$$u_{dq^{-1}} = \begin{bmatrix} u_{d^{-1}} \\ u_{q^{-1}} \end{bmatrix} = [T_{dq^{-1}}]u_{ab} = V^{-1}\begin{bmatrix} 1 \\ 0 \end{bmatrix} + V^{+1}\begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots (7)$$

Where,

$$[T_{dq^{+1}}] = [T_{dq^{-1}}]^T = \begin{bmatrix} \cos(\theta) & sin(\theta) \\ -sin(\theta) & cos(\theta) \end{bmatrix} \ldots\ldots\ldots\ldots (8)$$

Two decoupling cells are employed to determine the positive and negative sequence voltages V^{+1} and V^{-1} respectively. Which results in udq^{+1} and udq^{-1} components. which are approximately DC terms. Through decoupling of the sequence voltages, PLL works adequately under unbalanced faults as well, As the negative sequence voltage V^{-1} cannot be neglected. The DDSRF-PLL is suffered from high overshoot in the phase angle and frequency estimation, which appears at the moment of Fault [11].

D. Hybrid PLL:

A hybrid (dαβPLL) is a combination of the decoupling cells that are used in DDSRF-PLL (Fig. 5) to decouple the Sequence voltages and the αβPLL algorithm. To estimate the phase angle of grid voltage, which offers lower estimation overshoot instead of the algorithm that is

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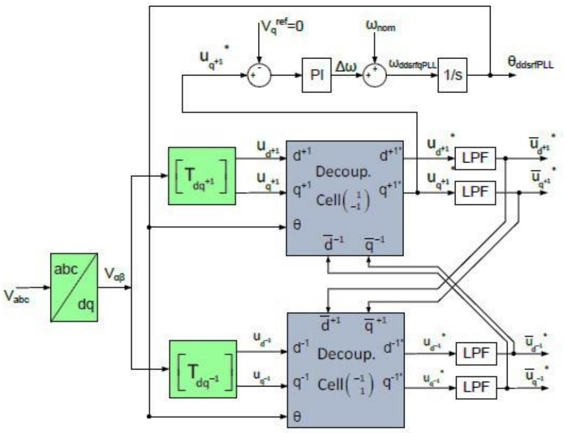

Fig: 6. Structure of Hybrid PLL

used in SRF-PLL (Fig:3). The hybrid PLL (dαβPLL) operates satisfactorily under unbalanced conditions. It also possesses the advantage of having a lower phase angle and frequency overshoot than DDSRF-PLL. Therefore, the Hybrid (dαβPLL) operates with much faster speed within the same frequency limits [14]. The structure of Hybrid (dαβPLL) is illustrated in Fig:6. It is designed to operate on three different time responses (fast-medium-slow) in order to keep reliability as compared with other PLLs.

IV. Conclusion

In this paper overview of Distributed Photovoltaic Generation is presented. Different synchronization schemes are listed, however the focus of this paper is aimed at the PLL techniques. A detailed study on different PLL schemes shows that SRF PLL gives better performance under ideal grid Conditions but faces problems during unbalanced faults. Enhanced Transfer Delay PLL is good with respect to overall performance. PLL based on Multi Harmonic Decoupling Cell is even faster in performance during Harmonic distortions, but it suffers from increased complexity. A new hybrid PLL gives better performance during unbalance condition with significantly faster speed. And it can also be designed for different time responses according to particular application.

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