Design of Efficient 3:8 Decoder Using CNTFET

[*]Diksha Manikkule, [#]Pravin Jaronde

[*]PG (M. Tech.) Electronics & Communication, [#]Assistant Professor, Department of Electronics & Telecommunication, D.M.I.E.T.R., Sawangi (Meghe), Wardha, India.

[*]dikshamanikkule@gmail.com, [#]pravinwj@rediffmail.com

Abstract— Binary logic is limited to only two states as it is two-valued logic. The ternary logic is the promising alternative to the conventional binary logic which is also called as trivalent logic. Energy efficiency and reduction in chip area as well as complexity plays an important role in ternary. Nowadays CNTFET device is more significant than the other due to higher channel mobility and also enhanced the gate capacitance. In CMOS, the complexity of an interconnect and chip area is increased as the number of function increases. This paper proposed an approach of using CNTFETs operate for faster and even consume less power in comparison with traditional MOS devices. Ternary decoder is designed using ternary logic and simulated in Tanner Tool software.

Keywords — CNTFET, Decoder, High Speed, Low Power, Ternary Logic.

I. INTRODUCTION

Another name for the three-valued logic is called as trivalent logic, which is also known as ternary logic allows more information to be transmitted as compared to binary. Complementary metal-oxide semiconductor (CMOS) technology is used by the PC microchip in transistors [2]. Digital circuits are synthesized, with an adaptable constraint, has been vigorously followed over the former few periods to the features of many design systems [2]. Logic circuits have been converted by high-level hardware depiction to develop several synthesis tools. The methodology for device synthesis supports the multivalued logic (MVL) [5]. The CMOS-based design performance is developed using the multivalued logic [3]. Multivalued logic (MVL) combined with incipient device carbon nanotube field effect transistor (CNTFET) for the development of new computing model [5].

The CNTFET consist of four terminals namely source, drain, gate and substrate as shown in fig.1. The carbon nanotube placed under gate region across two metal strips. One metal strip called as the source, and the other metal strip called as drain. The carbon nanotube acts as a channel between source and drain terminal. The substrate is made up of silicon oxide. The basic principle operation of CNTFET is the same as MOSFET where electrons are supplied by source terminal will collect these electrons. In other words, current is actually flowing from drain to source terminal. Besides, the current-voltage (I-V) characteristics of the MOSFET and CNTFET devices are alike. CNTFET also has P-type and N-type devices like MOSFET. However, unlike the MOSFET devices, P-CNTFET and N-CNTFET devices with same geometries have same mobilities (m_n=m_p) and as a result same drive capabilities. These unique characteristics are very consequential for simplifying the design and transistor sizing procedures of complex CNTFET-based circuits.

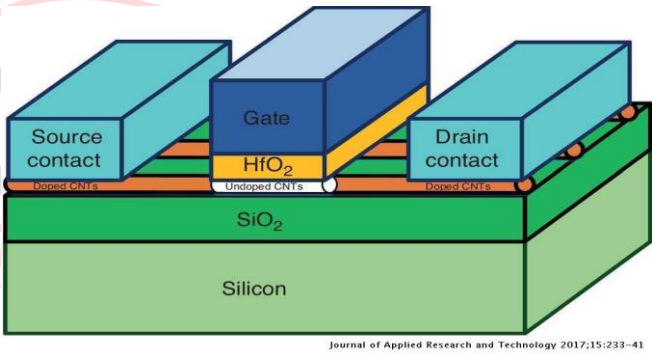


Fig.1: Structure of CNTFET

In general, CNTFET has higher ON current compared to MOSFET for the same OFF current. Due to the small molecular structure of the CNTFET device, scaling the future size, beyond what currently available advanced lithographic methods permit, is possible. In addition due to the fact that CNT does not have surface dangling bonds as Silicon, some other amorphous or crystalline insulators can be used instead of SiO_2 in the structure of CNTFETs. Ballistic conduction of the CNT decreases the power dissipation in the body of CNTFET, increases the speed of the device considerably and makes it suitable for low-voltage, low-power and very high speed and applications.

CNTFET is the best alternative for CMOS transistors [16] to continue the process of size reduction as of the similarities between CMOS and CNFET transistors have similarities in terms of electronic parameters. Fast implementation and less power CNFET based circuits are possible, which conquers backscattering and reason

 DOI : 10.18231/2454-9150.2019.0380 © 2019, IJREAM All Rights Reserved.

neighboring ballistic operation because of one-dimensional structure of the band. Transistor sizing is easy [6] for complex circuits using CNTFET. An alternative for MOS transistors is Carbon-Nanotube Field Effect Transistor (CNFET)s for achieving better performance at less power consumption [3]. For traditional MOSFET structure CNTFET use single carbon nanotube at the place of bulk silicon [2].

Usually digital computation is performed using binary logic. Increases the binary number logic input as per purpose, the chip area also increases [4]. Multiple-valued logic (MVL) systems are used [6] which permits more than two values. One of the examples of a multi-valued logic (MVL) system is the ternary logic with base 3 that carried out faster performance operation. Ternary logic reduces the area for higher bit order [4] and the number of required computation steps [15]. The proposed method focus on designing of ternary decoder using ternary logic to achieve less chip area with reduced complexity. Simulation is then performed using tanner tool to authorize their functionalities and confirmed their advantages in low power consumption with the high speed.

II. Related Work

The researcher [2] implemented a ternary logic circuit using 2:1 multiplexer. With 2:1 multiplexer, conversion of Binary Decision Diagram (BDD) can take place for switching each node in the BDD. Likewise, conversion of the ternary decision diagram (TDD) can take place using 3:1 Multiplexer. Ternary-Transformed Binary Decision Diagram (TBDD), is implemented using 2:1 multiplexer. Implementation of the synthesized circuit with the help of CNTFET, shows the result of transistors and compared with 3:1multiplexer.

The researcher [3] has designed an improved encoder used in the implementation of ternary logic circuits. Transformation of ternary signals to binary signals over binary gates and get the ultimate result of the ternary output of the encoder. To optimize parameters, such as energy usage, propagation delay, a suitable encoder is used for different output with different diameters of CNTs based on CNTFET, resulting in adder design.

The researcher [4] used CMOS technology to design a Ternary coded Decimal (TCD) adder circuit. The input and resulting sum is in the form of TCD form as TCD adder practices 3-bit Ternary coded Decimal (TCD). The design of the TCD adder boosted to less number of transistors and area benefit related to Ternary k map-based methods [4].

The researcher [5] designed a comparator using Carbon NanoTube Field Effect Transistor (CNTFET). CNTFET as well as CMOS comparator designs are compared to the improved performance.

The researcher [6] designed 6T SRAM cell and compared the performance CNTFET and CMOS. CNTFET has characteristics to outperform leakage in power saving, noise margin, speed and read static noise margin (SNM) as compared with CMOS cell. The simulation of the model shows for cell ratio and pull-up ration of 1 using the Berkeley predictive technology model.

III. Proposed Work

The performance of [5] the CNTFET devices are faster in comparison to that of CMOS devices. Therefore CNTFET based design shows considerably more improvement with less number of transistors and area benefit than that CMOS [4].

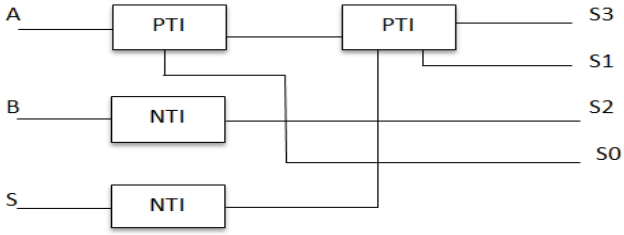


Fig.2: Block diagram of Ternary Decoder.

For designing a ternary logic circuit decoder-based methodology is used. Ternary logic is applied to for converting of ternary signals to binary signals. With the internal process binary signals are converted to the ternary decoder. Three inverters are there defined namely, Negative Ternary Inverter (NTI), Standard Ternary Inverter (STI) and Positive Ternary Inverter (PTI). The logic values assumed for different voltage levels are shown in Table II where, voltages 0, Vdd/2 and Vdd correspond to logic values 0, 1 and 2 respectively.

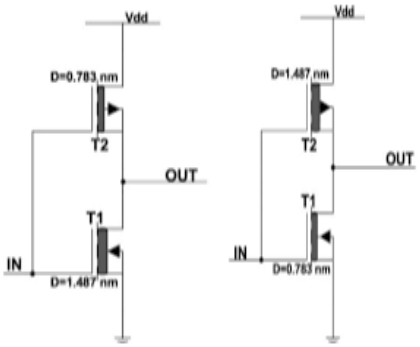
Table I: Ternary Inverters

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table II: Logic Symbol

Voltage level	Logic value
0	0
Vdd/2	1
Vdd	2

 DOI : 10.18231/2454-9150.2019.0380 © 2019, IJREAM All Rights Reserved.



(a) *(b)*

Fig.3: (a) NTI Gate and (b) PTI Gate

The PTI based mux is designed shown in fig.4. To continuously turn on the circuit negative power is connected to gate terminal of p-channel MOSFET. A variation of the L/W ratio of the p-channel MOSFET and n-channel MOSFET, then the resistance of the channel is changed. The output of the PTI depends on three input values.

The NTI based mux is designed as shown in fig.5. To continuously turn on the circuit positive power is connected to gate terminal of NMOS. The output of the NTI depends on three input values.

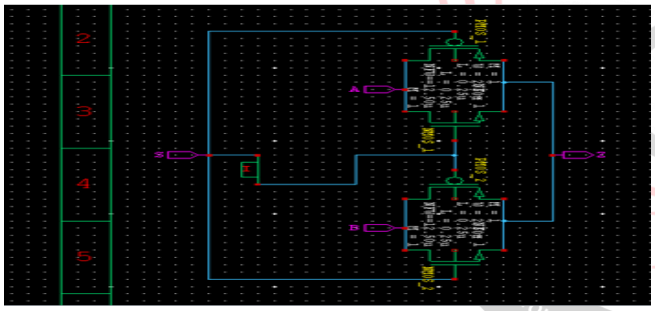


Fig.4: Implementation of PTI-MUX.

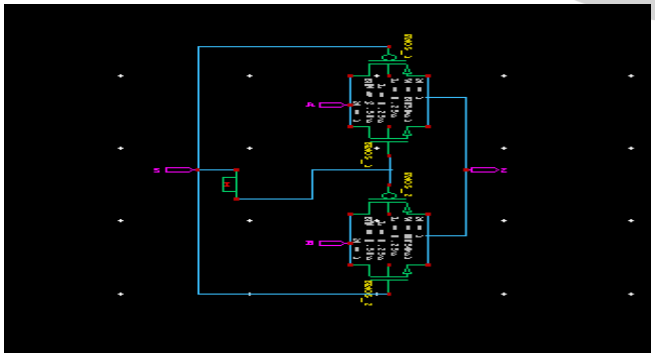


Fig.5: Implementation of NTI-MUX.

Design of 2:4 Ternary Decoder

The circuit is designed using PTI and NTI based MUX which requires two PTI and two NTI is shown in fig.6. The output of the decoder depends on input value which can produce more than one value as the use of ternary logic.

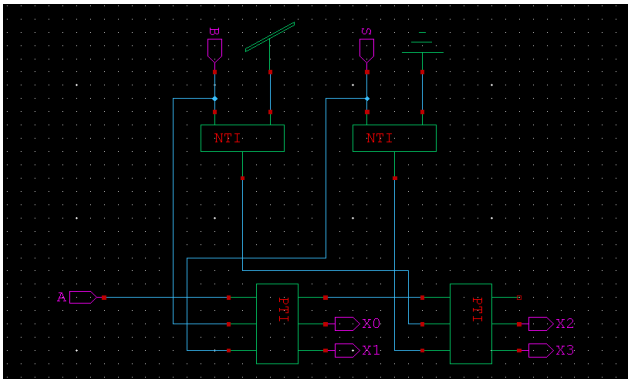


Fig.6: Implementation of Decoder.

Another circuit diagram of 2:4 decoder is shown in below fig.7. It consist of two NOT and four AND. Here NTI is being used as NOT gate. Implementation of this circuit shown in fig. 8. Similarly circuit diagram of AND gate is presented in fig.10. which is used in its implementation.

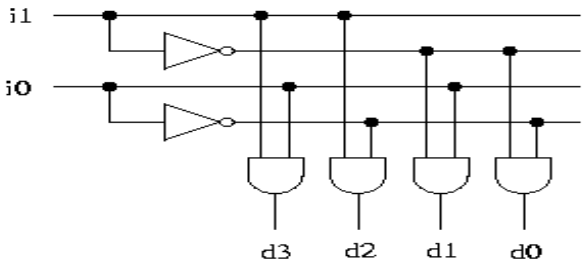


Fig.7: Circuit diagram of 2:4 Decoder.

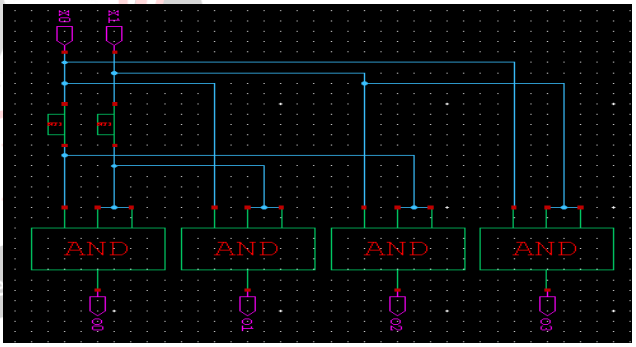


Fig.8: Implementation of 2:4 decoder.

Design of 3:8 Ternary Decoder

The 3:8 decoder circuit is as shown in below fig.10. Three NTI which act as NOT gate and eight AND are connected to make 3:8 decoder.

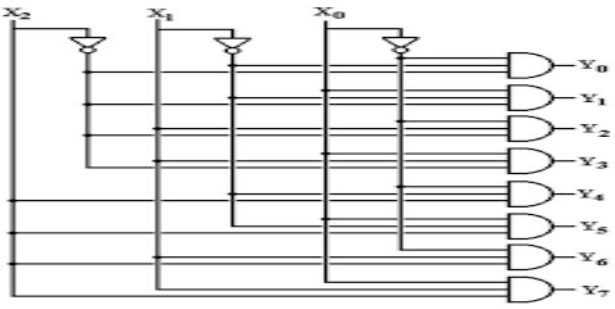


Fig.9: Circuit diagram of 3:8 Decoder.

 DOI : 10.18231/2454-9150.2019.0380 © 2019, IJREAM All Rights Reserved.

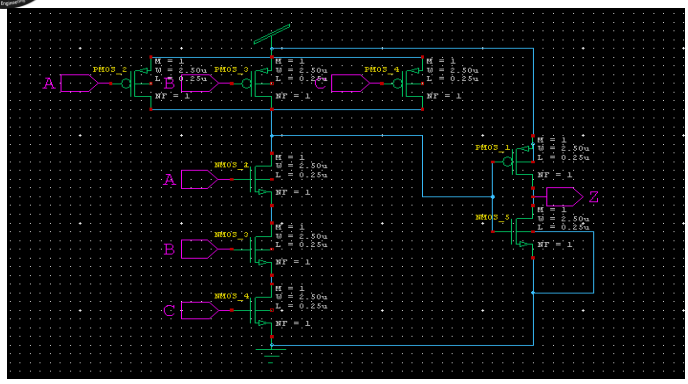


Fig.10: Circuit diagram of 3 input AND gate.

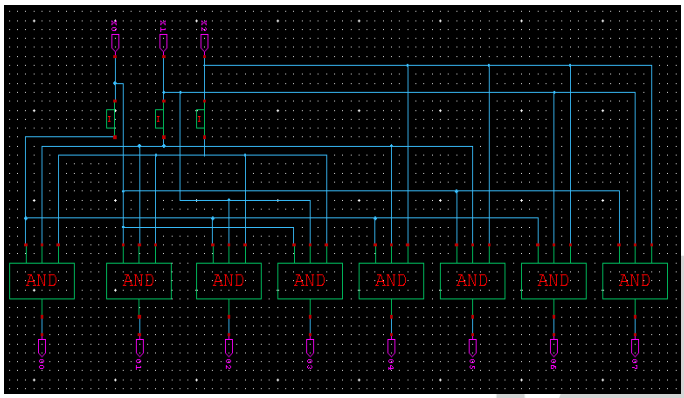


Fig.11: Implementation of 3:8 decoder.

IV. RESULT AND SIMULATION

The analysis of time delay, average power and simulation of PTI-mux, NTI-mux, 2:4 decoder, 3:8 decoder, full adder are depicted below:

Table III: Result of Time Delay

	Time Delay (ns)
PTI-mux	2.07
NTI-mux	2.02
2:4 Decoder	1.04
3:8 Decoder	1.82

Table IV: Result of Average Power

	Average Power (Watts)
2:4 Decoder	1.3030 (e-6)
3:8 Decoder	1.7456 (e-4)

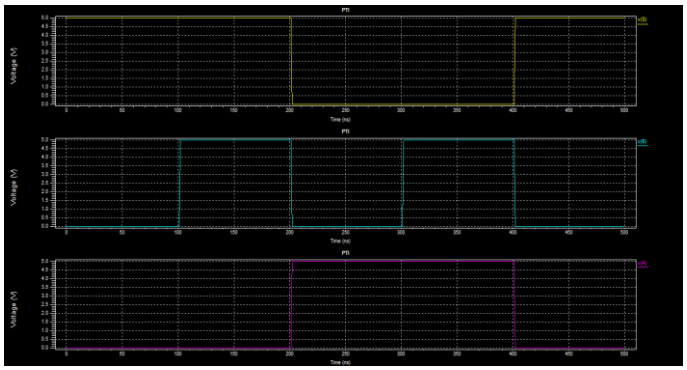


Fig.12.(a): Input of PTI MUX

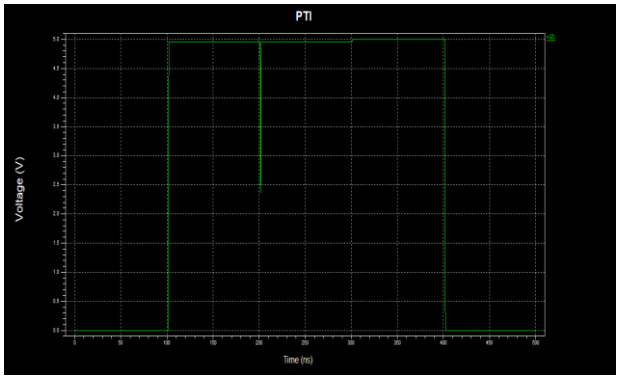


Fig.12.(b): Output of PTI MUX

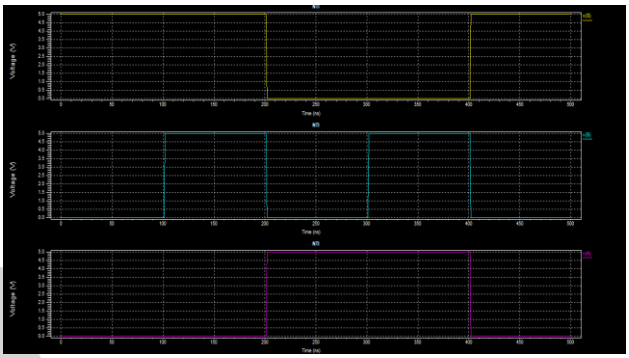


Fig.13.(a): Input of NTI MUX

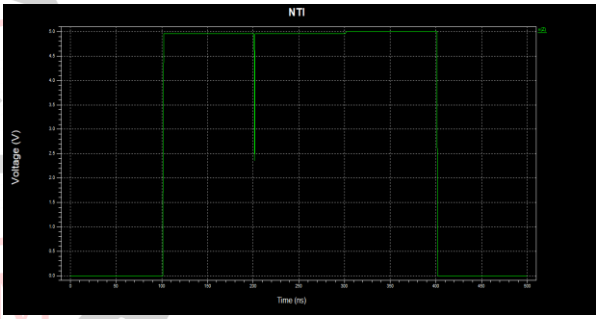


Fig.13.(b): Output of NTI MUX

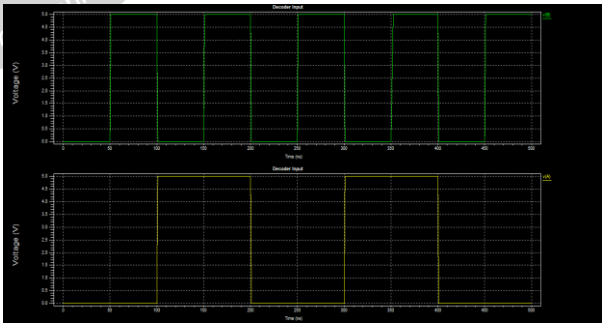


Fig.14.(a): Input waveform of decoder

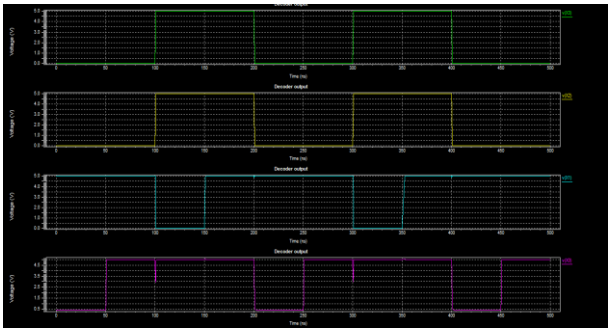


Fig.14.(b): Output waveform of decoder.

 DOI : 10.18231/2454-9150.2019.0380 © 2019, IJREAM All Rights Reserved.

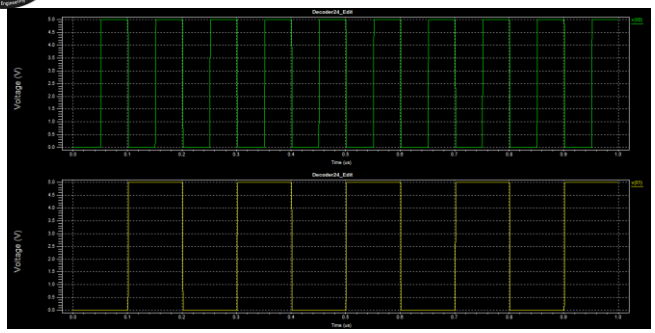


Fig.15.(a): Input waveform of 2:4 decoder.

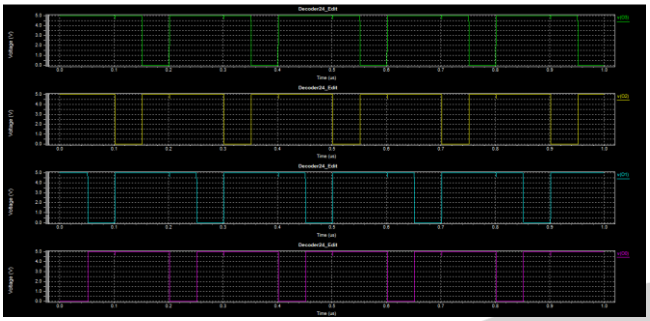


Fig.15.(b): Output waveform of 2:4 decoder.

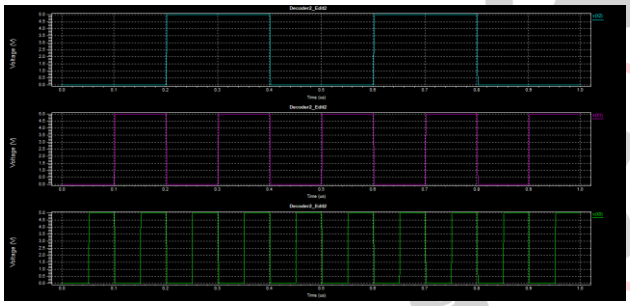


Fig.16.(a): Iutput waveform of the 3:8 decoder.

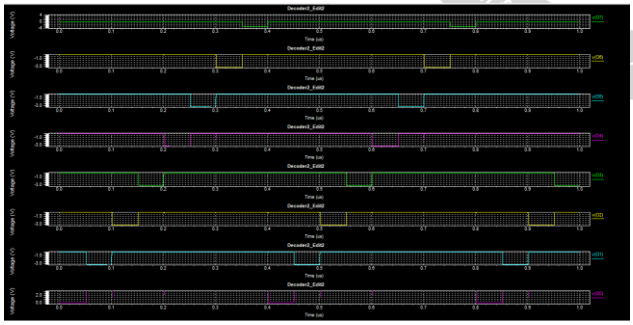


Fig.16.(b): Output waveform of the 3:8 decoder.

V. CONCLUSION

Ternary logic is that it reduces the number of computation steps over the binary. Time delay and average power is obtained through simulation is shown in the table III and IV. PTI-mux, NTI-mux, 2:4 decoder, 3:8 decoder has been designed using the ternary logic. All the simulation have been performed in Tanner Tool using 180nm CNTFET model due to excellent speed, small size, less complexity, less power consumption and very high speed and applications.

REFERENCES

[1] Diksha Manikkule, Pravin Jaronde "Design of Decoder Using Ternary Inverter", IEEE 5th International Conference for Convergence in Technology, MARCH 2019.

[2] Chetan Vudadha, Ajay Surya, Saurabh Agrawal, and M. B. Srinivas, "Synthesis of Ternary Logic Circuits Using 2:1 Multiplexers", IEEE TRANSACTION, 2018.

[3] Chetan Vudadha, Srinivasan Rajagopalan, Aditya Dusi, P. Sai Phaneendra, and M. B. Srinivas, "Encoder-Based Optimization of CNFET-Based Ternary Logic Circuits", IEEE TRANSACTIONS, MARCH 2018.

[4] J.Mounika, Mohd Ziauddin Jahangir, K.Ramanujam, "CMOS based design and simulation of Ternary Full Adder and Ternary coded decimal (TCD) adder circuit", IEEE 2016.

[5] Vipin V. Kashti1, Reena Monica, "Performance Analysis of CMOS Comparator and CNTFET Comparator Design", International Journal, April-2014.

[6] K. Kureshi, Mohd. Hasan, "Performance comparison of CNFET- and CMOS-based 6T SRAM cell in deep submicron", Article 2008.

[7] B.Srinivasu, K.Sridharan, "A Synthesis Methodology for Ternary Logic Circuits in Emerging Device Technologies", IEEE TRANSACTIONS, 2017.

[8] Vikash Prasad, Anirban Banerjee, Debaprasad Das, "Design of Ternary Logic Circuits using CNTFET", International Symposium, 2018.

[9] Manasi Muglikar, Dr. Rasmita Sahoo, Dr Subhendu Kumar Sahoo, "High Performance Ternary Adder Using CNTFET", Third International Conference, IEEE 2016.

[10] Sathish kumar, A. Swetha Priya, "Modeling of Combinational Circuits Based on Ternary Multiplexer Using VHDL", (IJCSE) International Journal, 2010.

[11] Mahsa Sedaghat, Mehdi Salimi, "Evaluation and Comparison of CMOS logic circuits with CNTFET", Article 2015.

[12] P. Saha, A. Jain and S.K. Sarkar, "A Comparative Study of CMOS and Carbon Nanotube Field Effect Transistor Based Inverter at 32 nm Technology Node", International Conference, March 2013.

[13] Md. Mehedi Hasan, "A General Method for CMOS Realization of any Logic Function in Ternary Computer System", IEEE 2007.

[14] R.Mariani, R.Roncella, R.Saletti, P.Terreni, "A Useful Application of CMOS Ternary Logic to the Realisation of Asynchronous Circuits", IEEE 1997.

[15] Vani H, Renuka Sagar, Rohini H M, "Multiplexer based Design for Ternary Logic Circuits", National Conference, 2015.

[16] Fazel Sharifi, Atiyeh Panahi, Mohammad Hossein Moaiyeri, Hojjat Sharifi & Keivan Navi, "High Performance CNFET-based Ternary Full Adders", IETE JOURNAL, 2017.

 DOI : 10.18231/2454-9150.2019.0380 © 2019, IJREAM All Rights Reserved.