Reversible Brent Kung Adder/Subtractor using Mach-Zehnder Interferometer Switch for Digital Optical Applications

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Abstract Reversible logic has received great attention in recent years due to its ability to reduce power consumption. Reversible logic improves energy efficiency, velocity of nano-circuits and the portability. Optical circuits are gaining much interest for their capacity to offer less delay and great efficiency. These optical circuits are designed using Semiconductor optical amplifier (SOA) based mach – zehnder interferometer (MZI) which plays a vital role in design of ultra fast all optical signal processing. these offer high speed, low power, switching time, ease of fabrication. We can construct irreversible circuits using reversible logic gates. Among all different types of adders, carry-look-ahead adders are fastest. Mach zehnder interferometer technique can be more helpful and advantageous for the digital optical fibre communications. This work presents new designs of reversible brent kung parallel prefix adders /subtractor for optical applications using 2's complement method. These designs are designed in verilog HDL using XILINX ISE Design suite 14.7 are synthesized and simulated using ISIM simulator.

Keywords — Carry look ahead adder, Logic Reversibility, MZI switch, Optical computing, Physical Reversibility, Reversible logic, Semiconductor optical amplifier.

I. INTRODUCTION

The history of VLSI can be dated back to the invention of transistors. In 1947, John Bardeen, Walter Brattain, and William Shockley all at Bell laboratories, also known as Bell Labs invented the point-contact transistor. The transistor's exponential growth count per chip was realized by Gorden Moore in 1965 and this became the famous Moore's law. It states that the transistor count per chip would double every 18 to 24 months. This law mainly focuses on two major forces.

- First, with the refinement of equipment the feature sizes are dramatically decreased for integrated-circuit technology.
- Second, to accommodate more number of transistors the die area is increased since the wafer's defect density has been reduced profoundly.

Reversal of time on quantum computers is also emerging so fast. For quantum computation, reversible logic is the backbone. Reversible logic used reversible gates for lossless information. In conventional computation the logic circuits are irreversible in nature. The inputs are not regenerated from outputs. So they dissipate a large amount of heat. According to Landeurs principle erasing a bit of information causes kTln2 joules of heat energy to be dissipated. In conventional logic bit of information may be erased which leads to loss of information and no chance to recover the inputs from outputs.

The original motivation towards the reversible computation is they dissipate less heat under ideal conditions, considerably less heat. According to the launder principle it is no heat. Considering the logic gate that performs a certain operation; information present at input will be lost at output. This lost information is dissipated into the environment. This is according to the principle of thermodynamics entropy. It is clearly understood that the charge present at input of the circuit gets grounded and flown away when it changes it state to obtain the output. Here a small amount of energy is taken away leaving to information loss. Whereas the reversible gates moves around the states and does not gets grounded. So as a result the loss of information is not possible leaving to energy conservation.

II. MACH – ZEHNDER INTERFEROMETER SWITCH

An optical MZI switch is a device which consists of two semi conductor optical amplifiers namely SOA 1 and SOA 2 along with three couplers namely C1, C2, C3 as shown in fig 1.as which most of the designs uses two couplers, one coupler for output and one for the input is used.

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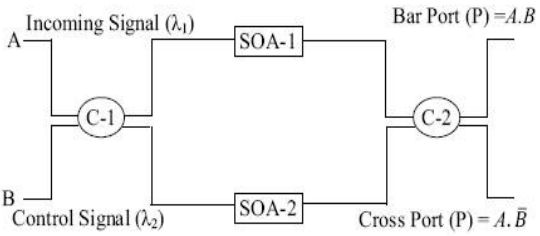

Fig 1: SOA based optical MZI switch

The inputs to first coupler are the incoming signals which is sent to both SOA1 and SOA 2.when control signal is sent to any one SOA either SOA1 or SOA2, it results in refractive index change which is given as $\Delta n = nI$. Here I is intensity of incident light and n is the refractive coefficient.MZI is balanced when control signal is absent. Change in refractive index causes the shift in phase of signal passing through SOA1. This results the incoming signal gets switched to bar port.

The optical MZI switch is shown in fig 1. It acts like a switch with the incoming signal being controlled by control signal. This incoming signal has the wavelength which is divided by the C1 coupler and propagates through SOA1 and SOA2 separately. When no signal is applied, the port is open. Due to this SOA1 and SOA2 were providing unsaturated gains. When a pulsed signal is applied to MZI through C2 providing most of signals to SOA1, this causes SOA1 to get into saturation mode resulting differential phase shift. In this mode SOA2 will be in unsaturation. "Switched state" takes place because of this phenomenon causing the output signal port 4 to switch to port 3 which is bar port. When no pulsed signal is given to MZI, "unswitched state" occurs resulting the output signal port4 which is cross port.

A. Beam Combiner (BC) and Beam Splitter (BS):

Beam combiner (BC) simply combines the optical beams while the beam splitter (BS) splits the beams into two optical beams. The optical cost and the delay of beam combiner and beam splitter are negligible [4, 6] and while calculating optical cost of a circuit, it may be assumed as zero.

B. Optical cost and delay:

As the optical cost of BS and BC are relatively small, the optical cost of a given circuit is the number of MZI switches required to design the realization. The optical delay is estimated as the number of stages of MZI switches multiplied by a unitΔ

III. REVERSIBLE LOGIC FUNDAMENTALS

Due to the anticipated failure of Moore's law around the year 2020, quantum computing will play an increasingly crucial role in building more compact and less power consuming computers. Due to this fact, and also because all quantum computer gates i.e., building blocks; primitives must be reversible. Reversibility in computing will have increasing importance in the future design of regular, compact, and universal structures and machines. (n,k) reversible circuits are circuits that have (n) inputs and (k) outputs and are one-to-one mappings between vectors of inputs and outputs, thus the vector of input states can always be uniquely reconstructed from the vector of output states. (k,k) reversible circuits are circuits that have the same number of inputs (k) and outputs (k) and are one-to-one mappings between vectors of inputs and outputs, thus the vector of input states can be always uniquely reconstructed from the vector of output states.

Conservative circuits are circuits that have the same number of values in inputs and outputs i.e., the same number of ones in inputs and outputs for binary, the same number of ones and twos in inputs and outputs for ternary. Conservativeness exists naturally in physical laws where no energy is created or destroyed. Reversible logic is a unique logic design style with equal number of input and output vectors. It follows one – to – one mapping between input and output. Unique output bits are derived from unique input bits. So it is easy to predict the desired input from desired output. This kind of prediction is not possible in conventional logic design, as many similar outputs are derived from different input bit combinations. In a reversible gate the outputs are 1's for exactly half of the inputs. In an n output reversible gate the output vectors are permutation of the numbers 0 to 2n-1.

The statement "information is physical", and the famous Eq. "information loss = energy loss" are appropriate. Based on this reason, different technologies have been investigated that implement reversible logic in hardware. Fully reversible digital systems will greatly reduce the power consumption through three conditions:

(1) **Logical reversibility**: the vector of input states can always be uniquely reconstructed from the vector of output states.

(2) **Physical reversibility**: the physical switch operates backwards as well as forwards

(3) the implementation using "ideal-like" switches that have no parasitic resistances.

A. Characteristics of reversible logic gates:

1.For a reversible logic gate fan out must be **one**. In the "forward" conventional logic synthesis combining wires is not allowed.In reversible logic synthesis branching wires will not be allowed since branching of a signal.If looked at in reverse, will appear to be as combining signals.

2.**Garbage output (gr):** it is defined as an output that is left unused. It is not the primary output for the gate. This garbage output is not connected to next level of any other gate.

3.**Ancilia input (AI):** it is defined as the input that is used to set the input fixed either to '0' or to '1'. This is used to

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equate the count of no of inputs and no of outputs for a gate. The basic an cilia inputs used are '0' and '1'.

4.**Quantum cost (QC):** it is defined as the no of reversible gates used in the design. Quantum cost represent the the total of 2 X 2 gates used.

5.**Hardware complexity:** it is defined as the number of logic operations used. This is also called as total logic operation. The main logic operations are NOT AND, EXOR.

To calculate the total logic operation for a logic circuit we use some special symbols like **α , β , γ.**

α Represents EXOR logic operation.

β Represents AND logic operation.

γ Represents NOT logic operation.

The total logic operation = **α + β + γ.**

All reversible gates can be constructed using reversible NOT gates and 2 X 2 reversible gates. The basic 2 X 2 reversible gates are controlled – V, controlled – V^+ and Feynman gate (FG). The internal circuit of controlled – V, controlled – V^+ are shown in fig2, fig 3, fig 4 respectively. The quantum cost of above mentioned gates are one.

Fig 2: NOT gate

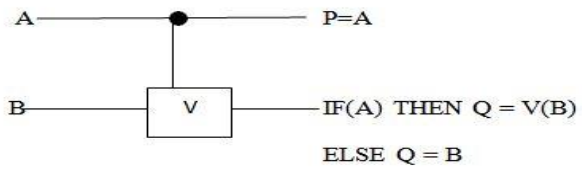

Fig 3: controlled – V gate

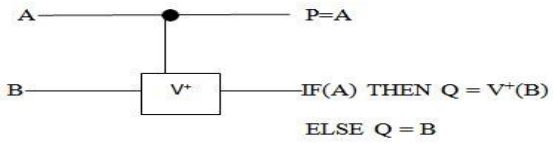

Fig 4: controlled – V^+ gate

IV. REVERSIBLE LOGIC GATES USING MZI SWITCH

A. Optical Peres gate (OPG):

The unique inputs 'A', 'B', 'C' of peres gate (PG) are uniquely mapped to outputs 'P', 'Q', 'R' in such a way that the functionality is P = A; Q = A ⊕ B; R=AB ⊕ C [6].

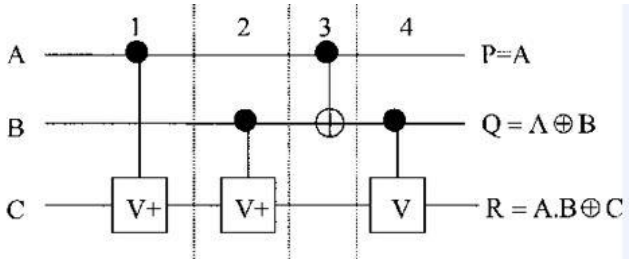

Fig 5: internal circuit of peres gate (PG)

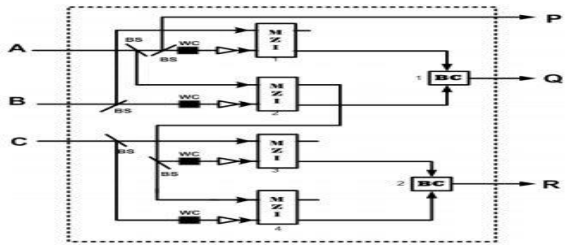

Fig 6: Peres gate using MZI switch

B. Optical Toffoli gate (OTG):

The toffoli gate [3]is also known as controlled – controlled NOT gate.if two inputs are set to logic '1', it inverts the third bit else all the bits remain same.The unique inputs 'A', 'B', 'C' of toffoli gate (TG) are uniquely mapped to outputs 'P', 'Q', 'R' in such a way that the functionality is P = A; Q = B; R=AB ⊕ C [6].

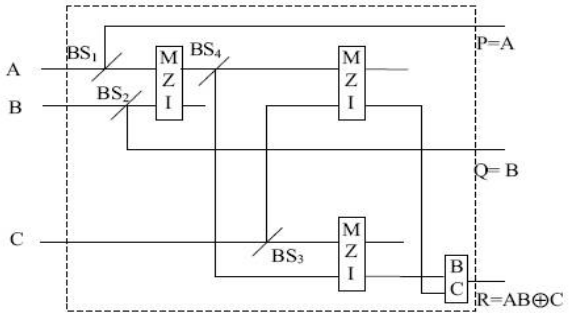

Fig 7: Toffoli gate using MZI switch

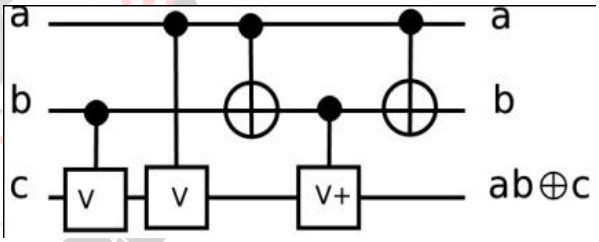

Fig8: internal circuit of toffoli gate (TG)

C. Optical Feynman gate (OFG):

The feynman gate is also called as controlled NOT gate.The unique inputs 'A', 'B' of Feynman gate (FG) are uniquely mapped to outputs 'P', 'Q' in such a way that the functionality is P = A; Q = A ⊕ B [6].

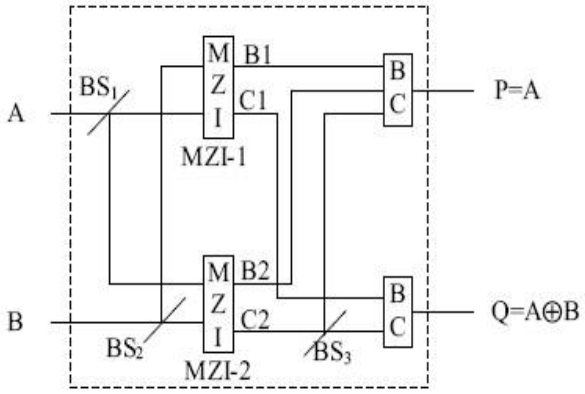

Fig 9: Feynman gate (FG) using MZI switch

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V. REVERSIBLE BRENT KUNG PARALLEL PREFIX ADDER

Adders are basic building blocks of common data path components. As the width of adder grows, delay for the carry to pass through stages dominates. So as to overcome this parallel prefix adders are in demand in this current VLSI technology. These adders are best in terms of area and time. These are particularly used to perform high speed addition of large numbers. This type of adders is described to prefix as the outcome of the operations performed during execution depending on initial inputs. The operations are performed parallel by segmenting into smaller pieces. There are lot of parallel prefix adders developed namely Han Carlson adder in 1987, kogge stone adder in 1973, sklansky conditional adder in 1960, brent kung adder in 1982, ladner fisher adder in 1980.

Parallel computing is a form of computation in which the calculations are carried out simultaneously, based on the principle that large problems are often divided into smaller problems and are solved concurrently in parallel. We have several types of parallel computation namely bit level, instruction level, data parallelism and task parallelism. Parallelism has been employed particularly in high speed computing for many years but it has grown lately due to main physical constraints preventing scaling. The main motive to go towards parallel computing is mainly the power consumption and heat generation by computers. This has become a major problem in recent years.

A. *Parallel prefix adders:*

In parallel prefix adders, binary addition is expressed in terms of carry generation Gi, carry propagation Pi, carry signal Ci and sum signal Si at every bit position. The signals are obtained by the equations below:

$$Gi=Ai+Bi \quad (1)$$

$$Pi=Ai \oplus Bi \quad (2)$$

$$Si= Pi \oplus Ci-1 \quad (3)$$

$$Ci=\{ \quad Gi , Gi+PiCi-1\} \quad (4)$$

Parallel prefix adders computes in three stages as shown in the below block diagram

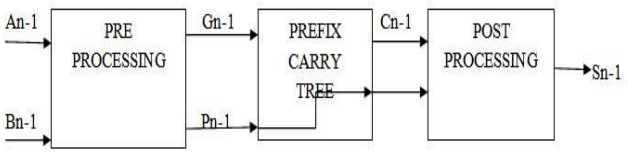

Fig 10: block diagram of parallel prefix adder

B. *Brent kung parallel prefix adder:*

Brent Kung adder is one of the types of parallel prefix adder. It resembles to the carry look ahead adder. The functionality is same to that of carry look ahead adder. This adder is proposed by Richard Peirce Brunt and Hsiang Te Kung in 1982. Among various parallel prefix adders, brent kung adder is shown to have better performance mainly in terms of delay and less chip area according to technology options. The carry generation and propagation in brent kung adder takes place parallel showing less delay. This adder has low fan-out from each prefix cell. But this adder has longest critical path. Accordingly this is considered as the better tree adder for minimizing wiring tracks, fan out, gate count.

C. *Stages of brent kung parallel prefix adder:*

Till now we have seen that on adding two numbers we get SUM and CARRY OUT with carry generate and carry propagate considering Cin as input. This operation better explained in the form of different stages. They are:

1. Pre processing stage
2. Carry generation stage
3. Post processing stage

These stages are shown in fig 11.

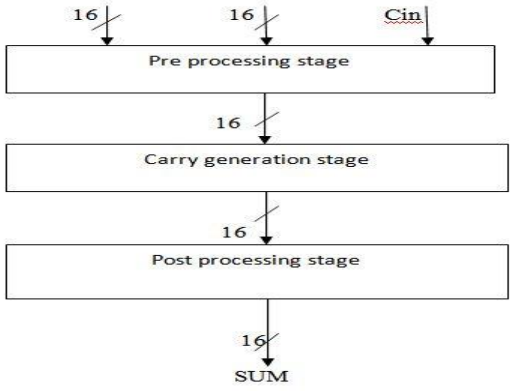

Fig11: stages of brent kung adder.

Stage 1:
In the first stage, the pre processing stage we obtain the bit wise group generate and bitwise group propagate signals.

Stage 2:
In the second stage, the carry generation stage we generate group propagate and group generate for carry signal.

Stage 3:
In the third stage which is the final stage, post processing stage using the carry bit and propagate signal we obtain the final SUM bit.

In pre processing stage the generate and propagate are obtained by the below equations with respect to their inputs.

Pi = Ai EXOR Bi

Gi = Ai. Bi

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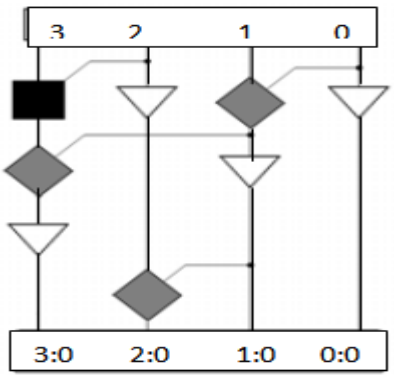

Fig 12: block diagram of 4 bit brent kung adder

In prefix stage group generate and group propagate are computed at each bit using the given equations. The black cell generates the ordered pair. The gray cell generates the left signal. Here a fundamental CARRY operator is used and is indicated by the symbol "o". This operator combines the generate and propagates signals by the below equation.

$$(gL , pL) \text{ o } (gr , pR) = (gL , + Pl . gr , pL . gr)$$

In the above discussion of carry look ahead adder we have noticed the group generate and group propagate signals. The generalized equations are as follows.

$$G_{i:j} = G_{i:k} + P_{i:K} \; G_{k-1:j}$$

$$P_{i:j} = P_{i:K} \; P_{k-1:j}$$

The generate and propagate signals are further grouped in different way to get the same correct carries. Based on the different ways of grouping the parallel prefix architectures are designed one among is Brent Kung adder with group generate and group propagate

$$Si = Pi . Gi\text{-}1: -1$$

$$Cout = Gn: -1$$

The Below 16 bit Brent Kung adder uses 14 BC'S and 11 GC's . this adder uses limited number of propogate and generate cells when compared to other types of parallel prefix adders.it takes less area and also has less wiring congestion. As it uses less BC's and less GC's the delay is less when compared to other parallel prefix adders.

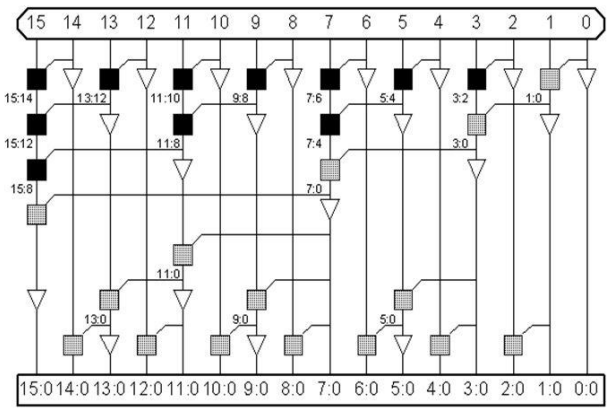

Fig13: block diagram of 16 bit brent kung adder

D. Design of reversible brent kung adder using complement method:

There are four types of design methods to perform both addition and subtraction is by complement methods namely

1. 1's complement
2. 2's complement
3. 9's complement
4. 10's complement methods.

We are designing the reversible brent kung adder using 2's complement method. This 2's complement method is obtained by taking 1's complement of bits and adding 1 to it. For subtraction operation to be performed the 2's complement of subtrahend is computed and is added to minuend.

$$A - B = A = 2'S \text{ complement of } B.$$

To get the two's complement of B number, B is inverted, then the value of 1 is added to the resulting value. It means:

$$A - B = A + B` + 1.$$

To design a reversible brent kung parallel prefix adder /subtractor. We assumed the input carry bit as the control bit. If the control bit is zero, the sum operation is performed, else subtraction by 2's complement method is performed. For this we use Feynman gate (FG).

The brent kung adder is designed using reversible logic gates. The black cell (BC) is represented using three peres gate (PG) to obtain propagate and generate of a carry.

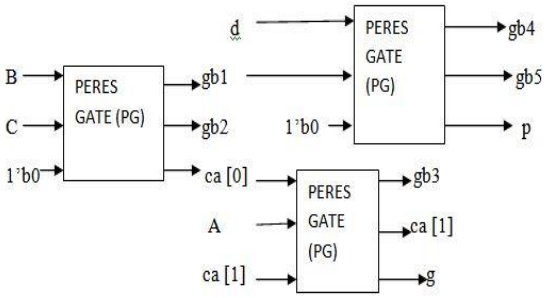

Fig 14: black cell representation using reversible logic gates.

The gray cell (GC) is represented with two reversible peres gate (PG) to obtain generate of carry. This generate is combined with carry to obtain the final SUM.

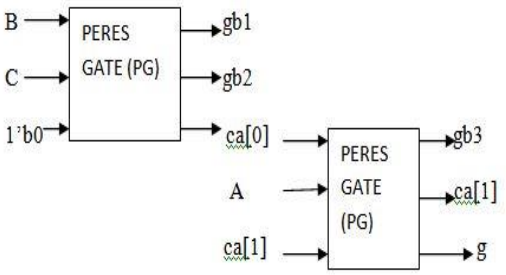

Fig 15: grey cell representation using reversible logic gates.

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This generate is combined with carry to obtain the final SUM.

VI. RESULTS

The device utilization summary of 4 bit reversible brent kung adder/subtractor using MZI switch is shown as below.

```
Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                      8  out of    960     0%
 Number of 4 input LUTs:               15  out of   1920     0%
 Number of IOs:                        14
 Number of bonded IOBs:                14  out of     83    16%
```

The delay of 4 bit reversible brent kung adder/subtractor using MZI switch is as below.

```
Delay:               9.997ns (Levels of Logic = 8)
  Source:            b<0> (PAD)
  Destination:       cout (PAD)

  Data Path: b<0> to cout
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5    1.106   0.607  b_0_IBUF (b1<0>)
     LUT3:I1->O            2    0.612   0.532  g2/c<1>11 (N11)
     LUT3:I0->O            5    0.612   0.690  gc1/gate2/Madd_q_lut<0>1
(co<1>)
     LUT4:I0->O            1    0.612   0.000  gc3/gate1/b_rnm0<1>12
(gc3/gate1/b_rnm0<1>1)
     MUXF5:I1->O           2    0.278   0.532  gc3/gate1/b_rnm0<1>1_f5
(gc3/gate1/b_rnm0<1>)
     LUT4:I0->O            1    0.612   0.000  gc3/gate2/Madd_r_lut<0>11
(gc3/gate2/Madd_r_lut<0>1)
     MUXF5:I1->O           1    0.278   0.357  gc3/gate2/Madd_r_lut<0>1_f5
(cout_OBUF)
     OBUF:I->O                 3.169          cout_OBUF (cout)
    ----------------------------------------

    Total                      9.997ns (7.279ns logic, 2.718ns route)
                                       (72.8% logic, 27.2% route)
```

The resultant wave form of 4 bit reversible brent kung adder/subtractor using MZI switch is

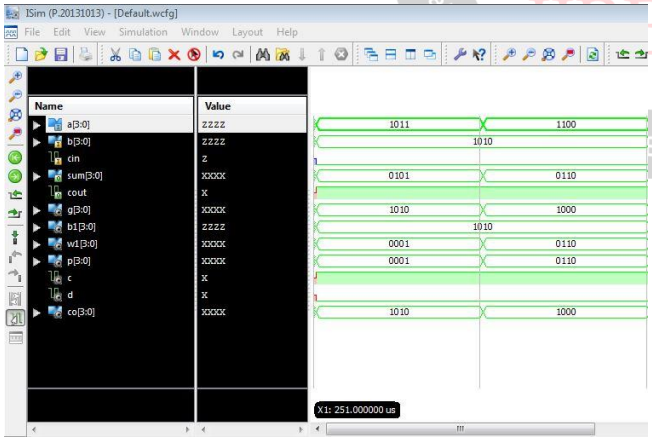

Fig 16: wave form of16 bit reversible brent kung adder/subtractor using MZI switch

The device utilization summary of 16 bit reversible brent kung adder/subtractor using MZI switch is shown as below.

```
Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                     50  out of    960     5%
 Number of 4 input LUTs:               90  out of   1920     4%
 Number of IOs:                        50
 Number of bonded IOBs:                50  out of     83    60%
```

The delay of 4 bit reversible brent kung adder /subtractor using MZI switch is as below.

```
Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 3824 / 17
-------------------------------------------------------------------------
Delay:               20.300ns (Levels of Logic = 18)
  Source:            b<0> (PAD)
  Destination:       sum<14> (PAD)
```

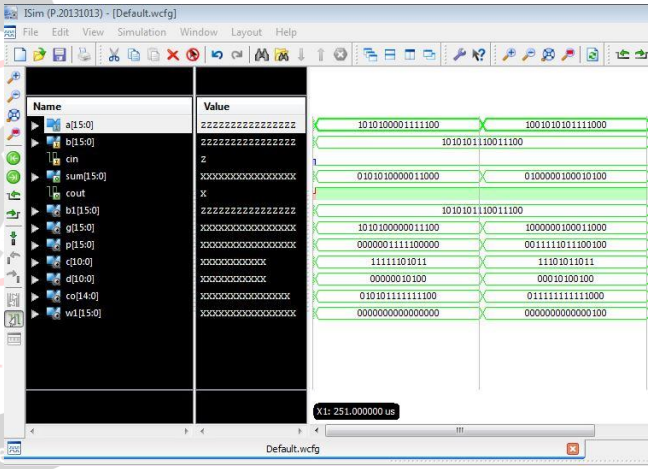

Fig 17: wave form of16 bit reversible brent kung adder/subtractor using MZI switch

Table: Table showing number of slices of device utilization summary

DESIGN	NUMBER OF SLICES
4 bit reversible brent kung adder/subtractor using MZI switch	8
16 bit reversible brent kung adder/subtractor using MZI switch	50

Table: Table showing number of 4 input LUT'S of device utilization summary

DESIGN	NUMBER OF 4 INPUT LUT'S
4 bit reversible brent kung adder/subtractor using MZI switch	15
16 bit reversible brent kung adder/subtractor using MZI switch	90

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Table: Table showing number of IO'S of device utilization summary

DESIGN	NUMBER OF IO'S
4 bit reversible brent kung adder/subtractor using MZI switch	14
16 bit reversible brent kung adder/subtractor using MZI switch	50

Table: Table showing number of bonded IO'S of device utilization summary

DESIGN	NUMBER OF BONDED IO'S
4 bit reversible brent kung adder/subtractor using MZI switch	14
16 bit reversible brent kung adder/subtractor using MZI switch	50

Table: Table showing delay of the design

DESIGN	DELAY(ns)
4 bit reversible brent kung adder/subtractor using MZI switch	9.997
16 bit reversible brent kung adder /subtractor using MZI switch	20.300

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