

# Design of OP-AMP Having High Gain and Reduced Power Consumption

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Dr. Jinsa Kuruvilla, Assistant Professor, MACE, Kerala, India, jinsak123@gmail.com Abstract : Design of circuits with low power and high gain is a difficult task to meet since these two requirements contradict each other. As the technology scales down the design complexity increases since the less power supply has to ensure the proper biasing of MOSFETs. The design of Op-Amp is now for specific application thus some parameters are compromised for the important one. The objective is to design an Operational amplifier suitable for biomedical application. Thus main target is to increase the gain and reduce the power consumption with lesser supply voltage . This paper proposes an Op-Amp circuit working with 1.5V supply voltage with high gain and reduced power consumption ( mW range).The designing technique and is implemented and analyzed using cadence virtuoso tool in 90nm technology.

Keywords —bio-medical, high gain, power consumption, Operational amplifier

## I. INTRODUCTION

Fundamentally an Op-Amp is a voltage amplifying device. It is designed to be used with external feedback components such as capacitors and resistors between its input- output terminals. the resulting operation or "function" of the amplifier is determined by these feedback components and depending on feedback configurations a variety of operations can be performed. An Op-Amp is designed for a specific application, often sacrificing unimportant aspects of the performance to improve the important ones.

Integrated electronics have been developed for small-scale amplification of the weak bioelectrical signals but they are having unacceptable noise levels or having higher powern End consumption. The integrated electronics must dissipate little power ensuring no tissue is damaged by heating. Frequency band of operations required for the electronic circuits varies with the type of bio potential signal. High level of system integration is required for a bio-potential system. Electrodes are placed on the surface of the skin for medical diagnosis of bio-potential signals. The commonly used bio-potential signals are ECG,EEG and EMG. Following Table I lists the rage of amplitude and frequency of these 3 commonly used signal. From the table it is clear that the amplitude range of the signals are very low which demand higher gain. But the frequency range of these signals are low. Hence cutoff frequency can be a lower value.

To have high gain, higher supply voltage is the need, but power consumption increases with supply voltage. Designing Op-Amp with lesser supply voltage is a challenge since biasing of all the MOSFETs have to be ensured.

 
 TABLE I. Amplitude and frequency range of commonly used biopotential signal

	Largest Peak	Frequency Range
ECG	1mV	0.5hZ-100Hz
EEG	100uV(when measured on the scalp) 2mV(when measured on the surface of the brain)	0.5Hz-100Hz
EMG	10mV Jewer	0Hz-500Hz

Moreover signal to noise ratio should be satisfactory with less supply voltage. Desired figure of merit of Op-Amp vary with application. High gain and less power is required for biomedical application where as higher slew rate is required for high speed application. simultaneously all parameters have to be optimized. An Op-Amp designed with low power ,high gain and also having lower power consumption is suitable for biomedical applications.

## **II. LITERATURE SURVEY**

Dynamic power consumption in the CMOS circuit is dependent to the supply voltage. So the supply voltage reduction helps in reduction of power consumption. By reducing the supply voltage the threshold voltage of the transistors is getting scaled down to maintain constant switching speed. But the reduction of the threshold voltage increase the leakage current exponentially. Signal to noise ratio is an important constraint that limits the use of small supply voltage [1]. This problem can be solved by the use of alternate MOSFET like floating gate MOSFETs, bulk driven MOSFETs and DTMOS [2].

An Op-Amp with floating gate input transistors can be used to increase the input common mode voltage range. For this



design, the input signal gets attenuated due to capacitive division which results in a poor gain[3]. Less gain bandwidth product and inferior noise properties are also the limitations for the same. Op-Amp with bulk driven transistors [4], overcame the threshold voltage limitation but it has lower transconductance value. The transconductance value lowers due to small control capacitance of the depletion layer, larger parasitic capacitance and higher input referred noise. The dynamic threshold voltage (DTMOS) transistor [5] based Op-Amp is preferred for low voltage, low power bio medical applications . the body and the gate of this DTMOS transistor are biased at the same potential . Hence it is capable of processing ultra low amplitude light signals and is used to build the front end receiver part of a Near Infrared Spectro Reflectometry (NIRS) device. The problem here is that the Op-Amp is susceptible to flicker noise (1/f), which makes it very harmful in low frequency bio medical applications because of its power spectrum and voltage offset.

Settling behavior of the op-Amp usually determines its accuracy and speed of the analog circuits[6]-[7]. High DC gain and a high unity gain frequency results in fast settling and high accuracy. The Gain of the op-Amp mainly depends on trans conductance and output resistance. Different techniques have been reported in literature to increase the DC gain. Cascading multiple stages and enhancing output impedance are two of the common methods[8]-[9]. Cascading multiple stages introduces stability issues. Frequency compensation techniques are needed to ensure the stability. Moreover cascading different stages cause limited output voltage swing. Gain boosting, cascading ,and applying positive feedback are the common methods for increasing the output impedance. Thus a proper design methodology is essential for an Op-Amp suitable for Enc biomedical applications[10].

## III. EXISTING ARCHITECTURE OF LOW POWER HIGH GAIN OPAMP

Sanjay Singh et.al [5] have proposed a low power high gain op-Amp suitable for biomedical applications which is having a differential input stage followed by an output common source stage. The schematic of the circuit is shown in Fig.1. In between the input and output stage a current mirror circuit is used. The design is done in a 90nm tanner eda tool. Output stage is having a compensation capacitor for the stability purpose. A current mirror is used to couple the first stage output to second stage. It is operating at 1.5v and is having gain of 93 db. The common source second stage ensures increased dc voltage gain and improved the output signal swing for a given operating voltage.

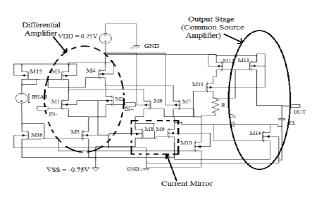
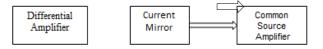


Fig 1: Schematic of LPHG Op-Amp.

In the system, high gain is obtained by using differential amplifier stage. The inputs are given as out of- phase to the common source NMOS connected in differential form. Owing to the differential configuration, the dc gain is high but at the same time this has the limitation of low output swing. To make better output-swing output stage in the form of common source stage is connected with compensation capacitor.

# IV.MODIFIED OPAMP CIRCUIT ARCHITECTURE

An operational amplifier is designed with the first stage being a differential amplifier followed by a current mirror circuit and then a common source stage. Differential configuration ensures immunity to noise. Single stage doesn't provide much gain, hence go with multiple stages. Fig.2 shows the block diagram of the proposed circuit. The current mirror circuit used here is responsible to sink the current in the input stage to output common source stage and is responsible for the higher gain. Output stage uses a miller compensation to provide the stability. To have higher current driving capability and lesser output resistance, the output stage bias current have to be increased. This can be achieved using this output configuration.

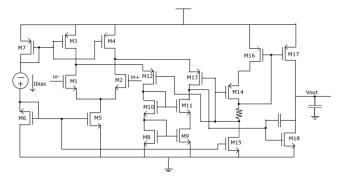


#### Fig 2: Block Diagram

Op-Amp circuits are mainly used in the feedback configuration. So the worst case happens with real time system have its stability dependency on the open loop Op-Amp configuration. When Op-Amp is designed with multiple stages that much pole is getting added to the circuit. Here comes the important of phase margin. Phase margin tell us how close the system is to oscillation. Amplifier generally use negative feedback. However if this is phase shifted by 180degree then it becomes positive feedback and the system will oscillate. One metric to decide how close to oscillation the system is finding out the phase



shift at unity gain and it is better to be below 180degree.In Operational amplifiers, the phase margin (PM) is the difference between the phase and 180 degree for an amplifier's output signal (relative to its input) at zero dB gain. In order to have better phase margin miller compensation capacitance is used.



#### Fig 3: Circuit Diagram of proposed Op-Amp

#### A. CIRCUIT DIAGRAM EXPLANATION

Fig.3 shows the circuit diagram of the proposed Op-Amp. M1,M2 -the n channel MOSFETs form the input differential pair with M3,M4 act as current source load.M5 carry the total current through the two branches. The current source load M3,M4 configuration helps in increasing the common mode range. M7& ad M6 are responsible for biasing the MOSFETs M3,M4 and M5 respectively. The current through the two branches are sinked to the final stage using the cascode current mirror circuit.M8,M9,M10,and M11 form the cascode current mirror circuit.M16 ad M14 are kept with the same aspect ratio. The total current of the first stage get amplified and is coupled to final M18 MOSFET. The current through M17 provide the bias current for M18 MOSFET.

#### **B.DESIGN METHOD**

In design setup the first step involved selection of basic structure of the Op-Amp. After setting the boundary condition dc biasing current is found out and then began to size the transistors and design compensation circuit. The specification listed in the Table II is set as boundary condition.

TABLE II. Design sp	ecifications for Op-Amp
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Power Supply	1.5 V
Differential mode gain	> = 90 dB
Unity gain bandwidth	30 MHz
Phase margin	60 degree
Slew rate	20 V/us
Power dissipation	< 100 uW

$$Av(0) = GMI *RI *RII *GMII$$
(1)

where Av is the dc gain of Op-Amp. GMi represents the transconductance of ith stage and Ri represents the equivalent output resistance of ith stage.Op-Amp transfer function can be derived from the small signal analysis and from the angle equation [8] .The compensation capacitance Cc is given by

$$Cc \ge 0.611CL \tag{2}$$

Where  $C_L\;$  is the load capacitance. Bias current is given by

I Bias = 
$$Cc * SR$$
 (3)

Where SR is the slew Rate.

MOSFET current (Id) in saturation region is defined by (4)

$$\mathbf{I}_{d} = \boldsymbol{\mu}_{n} \mathbf{C}_{ox} \frac{\mathbf{W}}{\mathbf{L}} \left( \mathbf{V}_{gs} - \mathbf{V}_{th} \right)^{2}$$
(4)

Here  $\mu_n$  is mobility,  $C_{ox}$  is oxide capacitance and W/L is aspect ratio of the MOSFET. This is the basic equation used for finding out aspect ratio. The following equation is used to find out aspect ratio of MOSFET M1 and M2.

$$\frac{W_{1}}{L} = \frac{W_{2}}{L_{2}} = \frac{g_{m1}}{\mu C_{m} * 2 I_{p1}}$$
(5)

Maximum of input common mode range,  $V_{\text{ICM}(\text{MAX}\,)}$  is given by

$$V_{ICM(MAX)} = V_{DD} - V_{SD3(SAT)} + V_{TN} (8)$$
 (6)

Where  $V_{DD}$  is supply voltage and is taken as  $1.5V, V_{SD(SAT)}$  is the source drain saturation voltage  $V_{TN}$  is the threshold voltage of NMOS. The aspect ratio of M3 and M4 can be found out using

$$\mathbf{V}_{ds3} = \sqrt{\frac{2*\mathbf{I}_3}{\mathbf{k}_p \cdot \frac{\mathbf{W}_3}{\mathbf{L}_3}}}$$

(7)

Minimum of input common mode range,  $V_{ICM(MIN\,)}$  is given by

$$V_{\rm ICM(MIN)} = V_{\rm DS5(SAT)} + V_{\rm GS}$$
(8)

 $V_{GS}$  is the gate source voltage.

Aspect ratio of M5 is computed from the following equation

$$\frac{\mathbf{W}_{s}}{\mathbf{L}_{s}} = \frac{2*\mathbf{I}_{s}}{\mathbf{k}_{n}\mathbf{V}_{sd5}^{2}}$$
(9)

Similarly, (10) and (11) give the relationships to find the aspect ratio of M8, M9 and M10, M11 respectively. $k_n$  is the process transconductance parameter.

$$\frac{\mathbf{W}_{s}}{\mathbf{L}_{s}} = \frac{\mathbf{W}_{s}}{\mathbf{L}_{9}} = \frac{2^{*}\mathbf{I}_{s}}{k_{n} \mathbf{V}_{sd8}^{2}}$$
(11)

Overall gain of the circuit is given by

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$$\frac{\mathbf{W}_{10}}{\mathbf{L}_{10}} = \frac{\mathbf{W}_{11}}{\mathbf{L}_{11}} = \frac{2*\mathbf{I}_{11}}{\mathbf{k}_{n} \mathbf{V}_{sd11}}^{2}$$
(12)

$$\frac{\mathbf{W}_{12}}{\mathbf{L}_{12}} = \frac{\mathbf{W}_{13}}{\mathbf{L}_{13}} = \frac{2*\mathbf{I}_{12}}{\mathbf{k}_{n} \mathbf{V}_{sd12}}^{2}$$
(13)

Since the MOSFETs M5,M6 and M15 are configured in current mirror circuit, the current through all these three MOSFETs are same. So they are having same aspect ratio. To compute aspect ratio of M14 and M16, (14) is used.

$$\frac{\mathbf{W}_{14}}{\mathbf{L}_{14}} = \frac{\mathbf{W}_{16}}{\mathbf{L}_{16}} = \frac{2*\mathbf{I}_{14}}{\mathbf{K}_{n} \mathbf{V}_{sd14}}$$
(14)

The gate to source voltage of M10 (VGS8) is given by

$$\mathbf{V}_{\rm esl0} = \mathbf{V}_{\rm DD} - 2\mathbf{V}_{\rm on} \tag{15}$$

M16 and M17 have same gate source voltage. So the current through M17 is proportional to current through M16. So,

$$\frac{\mathbf{W}_{17}}{\mathbf{L}_{17}} = \frac{\mathbf{I}_{17}}{\mathbf{I}_{16}} * \frac{\mathbf{W}_{16}}{\mathbf{L}_{16}}$$
(16)

The same current in M17 flows through M18. The relationship between trans-conductance( $g_m$ ) of transistors M1 and M18 is defined in (16). Using (16), aspect ratio of M18 is computed. These are given as,

$$g_{m18} = 10 * g_{m1}$$

Proposed Op-Amp is implemented in cadence virtuoso 90nm technology. The output MOSFETs are having larger aspect ratio to have high gain and high unity gain bandwidth.

The designed circuit diagram of high gain Op-Amp in 90 nm CMOS technology with a power supply of VDD =1.5 V is shown in Fig.4.



Fig.4 Schematic of modified circuit

Transient analysis has been done by giving 10uV sine wave as the input. The below figure shows the output sine wave obtained. The output peak to peak obtained is 800mV.

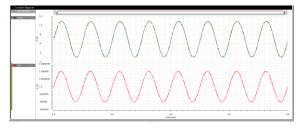


Fig.5 Transient output of modified circuit

AC analysis is done to find out the gain in dB, phase and unity gain band width. In the Ac Analysis frequency is selected as the sweep variable ranging from 100Hz to 100MHz. From the Figure.6, gain of about 98.7 dB, Unity gain bandwidth of 30.7 MHz, and phase margin of 48 degree are obtained.

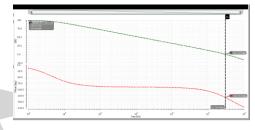


Fig.6 Bode plot of high gain Op-Amp in 90 nm

The gain obtained is 98.7dB,higher than the existing circuit. The unity gain bandwidth obtained is 30.7MHz which is close to the specification.

Slew Rate determines the speed of the circuit. It is the rate of change of output voltage with respect to time. To plot output slew rate waveform, negative terminal is shorted to output and a square waveform of 200mV to 1.5V amplitude and time period of 1uS is applied. The obtained slew rate is 24.5V/uS and is shown in Fig.7.

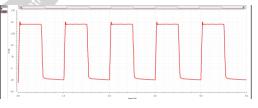


Fig.7 Slew rate plot of high gain Op-Amp in 90 nm

The below table shows the comparison between the existing and proposed circuit.

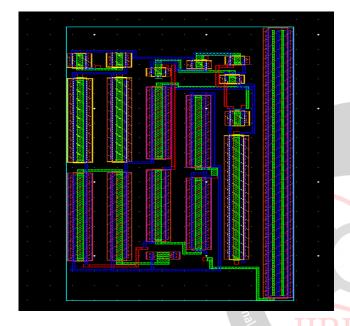
TA	BL	E	III.	DESIGN	SUMMAR	Y

	Existing Circuit	Modified Circuit
Power Supply	+/-0.75 V	1.5 V
Differential mode gain	93 dB	98.7 dB
Unity gain band width	11 MHz	30.7MHz
Phase margin	70 degree	48degree
Slew rate	20 v/us	24.5V/us
Power dissipation	1.83mW	2.4mW

(17)



Existing Op-Amp is having a high gain of 93dB with supply voltage of +/-7.5V.It uses a simple current mirror circuit between the first stage and common source stage to increases the gain. The proposed circuit uses a cascode current mirror stage instead of simple current mirror. Cascode current mirror is having a higher gain which causes an amplified current to flow through the final stage. The modified circuit is having a higher gain compared to the existing but it is having higher power consumption. Even though it satisfies the specified Objective. From the above discussion the modified Op-Amp circuit is suitable for biomedical application. The figure below shows the layout of proposed Op-Amp



# Fig.8 Layout of the modified circuit

## **VI. CONCLUSION**

Today's amplifier selection is quite complex, due, in part, to n Engi [9] P. E. Allen and D. R. Holberg, CMOS Analog Circuit the variety of system design requirements and the multitude of circuit configurations. Every application requires a different combination of specifications, and the number of available amplifiers continues to expand to fit those needs. An Op-Amp is designed for a specific application, often sacrificing unimportant aspects of the performance to improve the important ones. For biomedical application, the Op-Amp should have a high gain and low power consumption.

The proposed Op-Amp is having high gain and high unity gain bandwidth compared to the existing one. Proposed Op-Amp have higher power consumption compared to the existing one, but it is less than the specification. So the proposed Op-Amp is suitable for biomedical application.

## REFERENCES

[1] Y. Chih-Jen, C. Wen-Yaw, and C. M. Chen, "Micropower low-offset instrumentation amplifier IC design for biomedical system applications," IEEE Trans. Circuits and Systems I: Regular Papers, vol. 51, pp. 691-699, 2004

- [2] M. Santhanalakshmi and P.T. Vanathi, "A 1.2V improved operational amplifier for bio-medical Applications", Int. J. Biomedical Engineering and Technology, Vol. 9, No. 4, 2012.
- [3] Raisanen-Ruotsalainen. E, Lasanen. Κ. and Kostamovaara.J. (2000) ""A 1.2V micropower CMOS op amp with floating-gate input transistors", Proc. 43rd IEEE Midwest Symp. Circuits and Systems, Vol. 2, August, pp.794–797.
- [4] Lasanen, K., Raisanen-Ruotsalainen and Kostamovaara, J. (2000) ,"A 1V 5µW CMOS op-amp with bulk driven input transistors", Proc. 43rd IEEE Midwest Symp. Circuits and Systems, Vol. 2, August, pp.1038-1041
- [5] Achigui, H.F., Fayomi, C.J.B. and Sawan, M. (2003), "A DTMOS-based 1V op-amp", Proc. ICECS, Vol. 1, December, pp.252–255.
- [6] Sanjay Singh Rajput1, Ashish Singh2, Ashwani K. Chandel, and Rajeevan Chandel, "Design of Low-Power High-Gain Operational Amplifier for Bio-Medical Applications" IEEE Computer Society Annual Symposium on VLSI, pp.355-360,2016.
- [7] Er. Rajni, "Design of High Gain Folded-Cascode Operational Amplifier Using 1.25 um CMOS Technology", International Journal of Scientific & Engineering Research, Volume 2, Issue 11, November-2011.
- [8] B. Razavi , Design of Analog CMOS Integrated Circuits, 2002.

Design, Book, Oxford University Press, 2002.

[10] H.R.Dehsorkh, N.Ravanshad, R.Lotfi, K.Mafinezhad, and A. M. Sodagar,"Analysis and design of tunable amplifiers for implantable neural recording application, "IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1, pp. 637-647,2011