Study and Implementation Of DVFS Technique for Processor Power Reduction

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Abstract- **We can call this decade as the era of battery operated devices, so we need best speed with low power consumption but the quick battery drain out is the major issue, the power dissipation is one of the main reason for this drain out, so we are using Dynamic Voltage and Frequency Scaling (DVFS) to reduce this dissipation by scaling voltage and frequency based on the workload on the processor to achieve goal of energy saving. The Simulink simulator results confirm the theory.**

Keywords- Processor, Workload, Power dissipation, DVFS, Power reduction, Simulink.

I. INTRODUCTION

In the world 70-80% of people directly or indirectly depends on battery operated devices like mobile phones, tabs, laptops etc. [1].We expect these devices to perform multiple and complex tasks in an effective way, if we run these systems at high speed it consumes high power and this leads to high power dissipation. In the battery operated devices this is the major issue, because this dissipation is responsible for quick battery drain out and this limits the heavy use of this devices in competitive way and Power dissipation tends to system hot then its components tend to fail easily and this fail doubles for each 10 degree increase [9]. According to [13] if we are considering sources of power dissipations they are as follows

The Static dissipation of power is given as

$$P_{static}= (V_{dd} * I_{Leakage}) \text{------------------------------------} (1)$$

The Dynamic dissipation of power is given as

$$P_{dynamic}= \alpha\left(C_L * V_{dd}^2 * f\right)\text{------------------------------} (2)$$

The Short circuit dissipation of power is given as

$$P_{sc}=\left(\frac{KW}{L} * \frac{1}{2}V_{dd}^3 \left(1 - \frac{2V_t}{V_{dd}}\right)^3 f\right)\text{--------------------} (3)$$

In the equation 1, 2, 3, where V_{dd} is supply voltage, V_t is threshold voltage, C_L is load capacitance, k is dependent constant, W/L width length ratio, f is the frequency of operation and $I_{Leakage}$ is the leakage current.

From all these equation it clears that all type of power dissipations are depends on supply voltage, so by reducing supply voltage we can reduce power dissipation this is possible by DVFS technique.

II. RELATED WORK

In [5], proposed the power aware task model for dynamic frequency scaling on embedded system, which is implemented on the Linux operating system. We can apply this method at where no urgency task executing and memory related instructions are executing because the time is wasted in these two.

In [3] proposed a system, in that they try to reduce the power of processor, for that they used the concept of doing the dynamic frequency scaling of the low priority tasks and task migration on high priority tasks. So they can facilitate high priority tasks effective execution, for this the low priority tasks performance is sacrificed. In this they achieved 5-6% power reduction with just 0.24% performance loss of high priority task.

In [10] proposed the application driven frequency scaling methods for improving efficiency, in this there ultimate goal is to satisfy its users not to execute a particular number of instructions per second, if the CPU uses the low frequency for the execution then it is not an issue if it is non noticeable by the user, to verify this they used the Lenovo think pad laptop of core duo, 2GB ram, 4 frequency states.

In [8] proposed the low power architecture design technology for high performance processors, in this they used the method of reducing switching activity by gray code addressing instead of normal, because it is only one bit change from address to address.

In [7] proposed the method, in that, they use the concept of clustered clock gating and macro cell reusability at the RTL level this reduces dynamic power consumption without loss of performance. This leads to the 37% of power saving, which is very big optimization in micro controller.

In [2] proposed the algorithm called VI-LAMCS, in that they implemented the hybrid task allocation method using technologies like worst fit decrease, first fit decrease etc. This optimizing the static and dynamic energy of cluster based multi core processors with separate clock and supply voltage for each cluster. In that algorithm initially selects one frequency then reducing it step by step for optimal one. It handles hard deadline periodic task with soft real aperiodic tasks while optimizing the energy consumption. It uses unused capacity of cores for both periodic and aperiodic tasks.

In [4] proposed the Dynamic power management for low power RISC embedded system on SoC. In that they proposed the new architecture for the RISC processor, for that they used Verilog language for writing code and Xilinx ISE 12.3 tool for synthesis. The main concept of this implementation is when not in use just turn off it. The RISC processor core operates at maximum speed of 401.881MHz and use power of 1440 mW. The overall SOC (System-on-Chip) module operates on maximum Frequency of 214.508MHz.

In [6] made survey on different frequency scaling methods to check the security threat and amount of data loss due to dynamic frequency scaling. Then after they came to the conclusion that the data loss is not only depends on frequency scaling, it also depends on the hardware and version of operating system used.

III. DVFS TECHNIQUE ANALYSIS

90-95% of dissipation is during the run time [4]. If we reduce supply voltage we can reduce power dissipation. DVFS allows to scale voltage during run time. [14].

Dynamic scaling of voltage and frequency means dynamically varying the frequency and voltage based on the present workload on the processor to achieve the goal of power reduction.
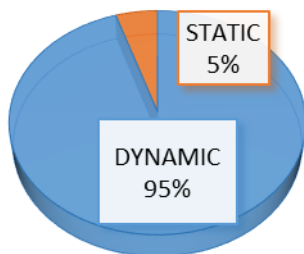

Figure 1.Power dissipation analysis

We can conclude that in a system if we consider the dissipation only 5% is due to static and remaining 95% is because of the dynamic activity, is shown in figure 1.

Hence it allows optimization of power and energy consumption by altering supply voltage and frequency, in simple way we can say that it saves dynamic power at run time. By doing this we have to compromise little bit with throughput, this compromise is manageable because power reduction is our primary consideration and user satisfaction is very important rather than working at high speed of processor. In this voltage and frequency pair is applied in open loop manner as determined at the time of design by keeping sufficient margin with guaranteed operation at entire work condition.

In the figure 2 its clearly shows that both voltage and frequency are internally related when the voltage drops, frequency also drops with linear relation at the beginning after certain voltage it drops dramatically.
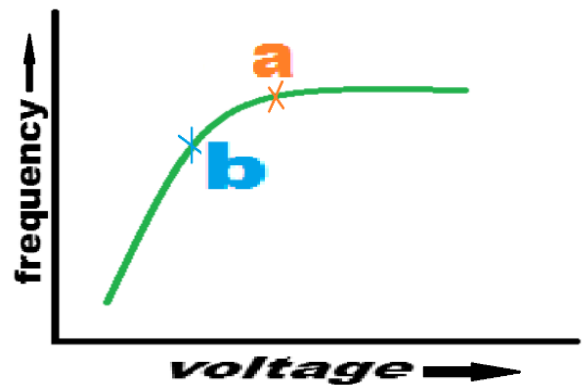

Figure 2. Voltage frequency relation

The Figure 2 graph is not identical for all the processor because practically not all the processors are same due their chip properties, process, design and performance on the various temperature conditions, so we are consider the figure 3 which is more practical approach. In nature it is called as process voltage temperature (PVT) spread [6].

In the real world 96% of processors lay between these two curves [14], the main reason for these curves are dynamic changes in the chip which is also classified into fast and slow changes.

The slow changes are like Die drain voltage fluctuations, temperature variations, internal temperature hot spots, fast changes like PLL Jitter, clock tree jitter etc.

Basic DVFS using Frequency and voltage relation can be explained as follows, for that we no need to run processor at common and fixed frequency and voltage throughout, because tasks to the processors are time varying criteria, we can reduce or vary these two based on our requirements. When we reduce frequency and voltage, the power consumption and power dissipation automatically comes down, figure 2 explains this basic DVFS method.
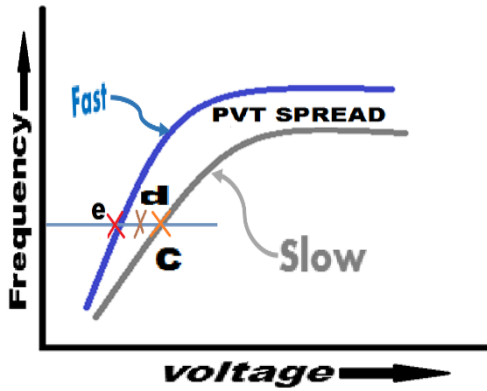
Figure 3. Voltage frequency relation with PVT spread.

Let us consider one processor running at the voltage a, as shown in the figure 2. Suppose we push down this processor to the voltage b**,** then we get additional saving of (a-b) difference. We are initially try to control voltage because it is easy to control, we have voltage regulators for that. But in this type we have compromise with the performance there must be some lose in it. When we are doing this the frequency also comes down automatically.

For the other scenario consider the figure 4 in that two processors running at c and d**,** they are operated at same frequency, but at different voltage. In case if we push down the voltage of these to operate at point e, then there is no change in the frequency, then there is no change in the performance but saving in the voltage. Hence automatically power dissipation comes down without performance loss, it called as over clock [14]. Because performance increases with reducing voltage, in other word we can say that we can move from the slow performance to fast performance processor by varying only the voltage. Let us consider the figure 4 in which a work load is 100% and time required by CPU to complete this task is t_1 and the power dissipation is given by P_1, for all that we have deadline D. Then the energy consumed to complete this task is the product of both power and time.

$$E = P_1 \times t_1 \text{--- (4)}$$
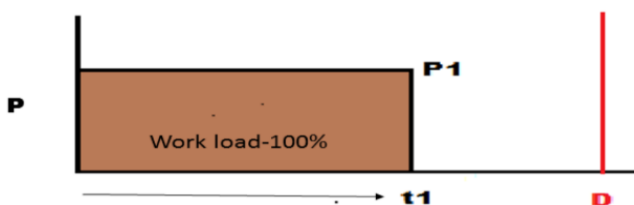

Figure 4. Workload of 100%.

Suppose the workload is 50%, then the computational time is also reduced to half. Then energy consumed is given by

$$E_2 = P_1 \times t_{1/2} \text{--(5)}$$

But the power dissipation is remain same, because the CPU runs simply for the remaining duty cycle, this is shown in the figure 5. In this case no voltage and frequency scaling takes place.
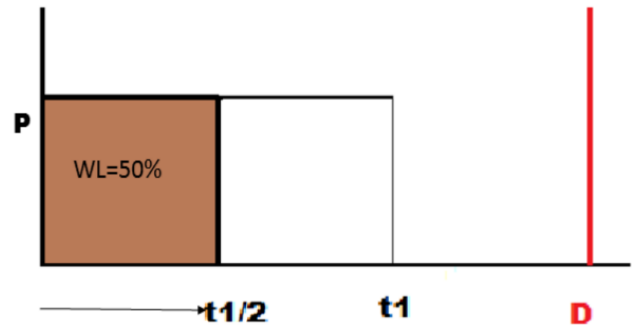

Figure 5. Workload of 50% with same dissipation.

Now let us consider the figure 6 with frequency scaling then the CPU works with low frequency.
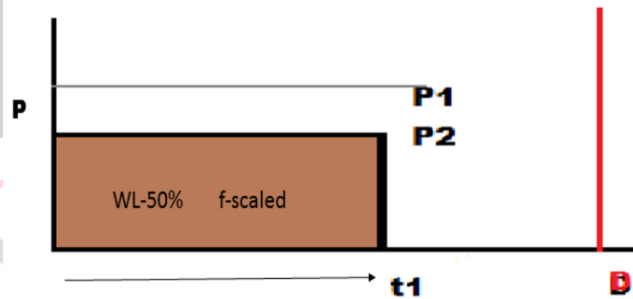

Figure 7. Workload of 50% with frequency scaled

Now it clearly shows that, there is a reduction in the power dissipation, but the energy consumes is same as equation (5).

$$E_3 = P_2 \times t_1 \text{--- (6)}$$

Then we can conclude that both equation5 and 6 are identical, and also we can conclude that with only frequency scaling we can reduce power dissipation, but not energy this also impact on the CPU operation. If the frequency is scaled the voltage required for the operation is also reduced then we can easily scales down the voltage as we required. In the figure 7 it clearly shows the effect of both voltage and frequency scaled, the energy consumed is given by

$$E_4 = P_3 \times t_1 \text{--- (7)}$$
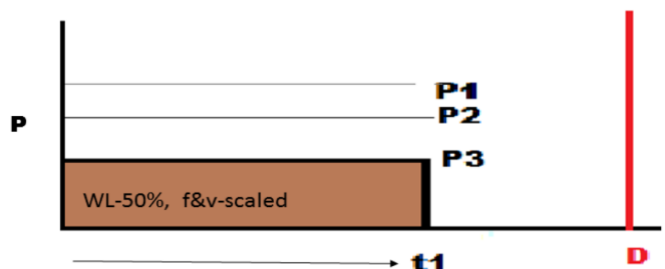

Figure 7. Workload of 50% with frequency and voltage scaled.

This type of methods are very useful for the battery operated devices, because there is a linear relationship between the power dissipation and battery life.

IV. PROPOSED WORK

In the proposed work, for the processor instead of giving supply voltage directly, we are given through the control loop. This control loop works based on the work load to the processor.
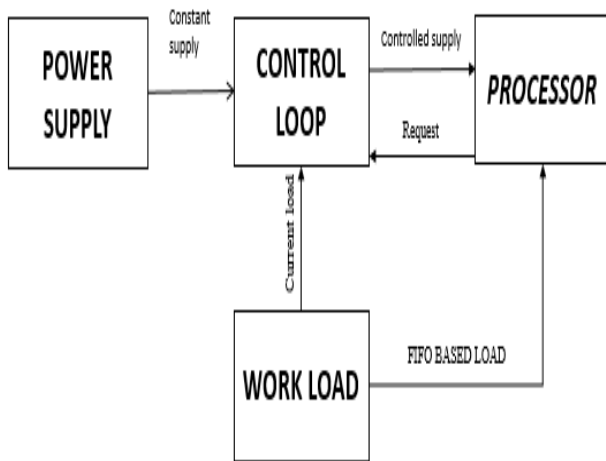

Figure 8. Proposed DVFS system.

We know that work load to the processor is time variable, hence this control loop take the present work load as reference.

When new work is arrived to the processor on the basis of First In First Out (FIFO), it sends request to the control unit for new voltage, then in control unit it consider the constant supply voltage and present work load, it produces the new predicted controlled voltage.

This prediction is based on an infinitesimal perturbation analysis (IPA). IPA can provide sensitivity information that yields a first-order approximation of the system performance metrics as a function of the parameters.

The performance metric to minimize is the average voltage per job, given by

$$J[\theta] = \omega P[\theta] + S[\theta] = \omega C_2 \left[V_t / (1 - C_1 / \theta) \right]^2 \quad \text{------------------(8)}$$

- θ is the average service time of a job and it is a function of the input voltage V. This finds the optimal value of θ also yields the optimal value of V.

- ω is a weighting constant.

- $P[\theta]$ is the average energy consumption of a job in Joules.

- $S[\theta]$ is the average time for jobs, which measures quality of service.

- C_1 and C_2 are device-dependent constants.

- V_t is the device threshold voltage.

This average voltage is given as supply voltage to the processor, in this work we are using limited supply based on work load, then the power consumption is decreased, then automatically power dissipation is reduced.

V. RESULTS

The proposed DVFS work has been simulated using Simulink simulator, in the simulator we simulate AT90S8535 DVFS supported microcontroller, voltage controlled oscillator (VCO), which is the main controlling block of the work, which produces new controlled voltage supply to the processor. Voltage Trans Conductance Device (VTD), which shows how the device operating voltage change with change in supply voltage and power supply. The following waveforms are obtained.

For voltage request of 2 volt which is the minimum voltage request from the processor, output of VCO in figure 9 shows that it produces the 2v constant supply , VTD shown in figure 10 clears that how operating voltage change to 2v and power dissipation shown in figure 11.

Also for voltage request of 4.3 volt, which is the average voltage request from processor, the output of VCO, VTD and power dissipation is shown in figure 12 13, and 14 respectively.
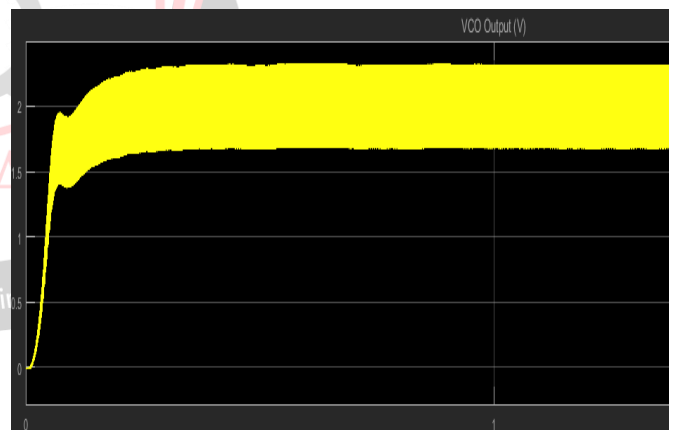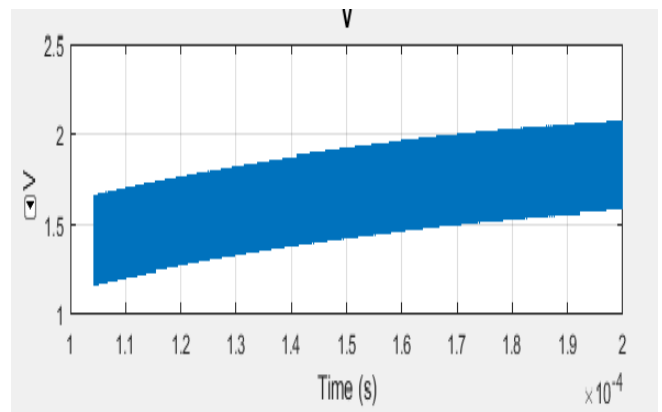

Figure 9. VCO output when voltage request is 2v.
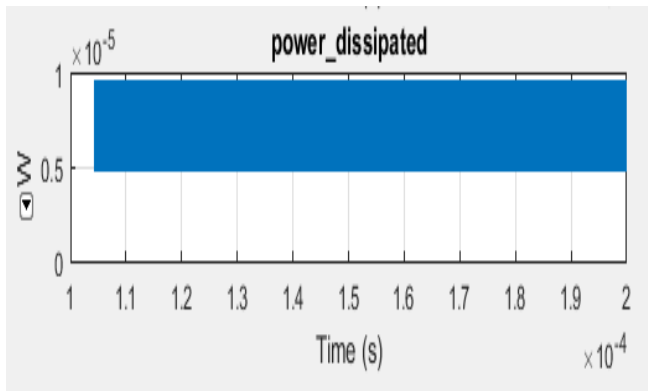

Figure 10. VTD output when voltage request is 2v.

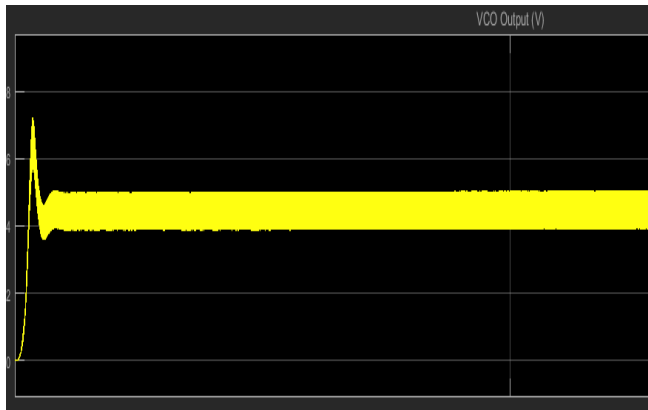**Figure 11. Power dissipated when voltage request is 2v.**

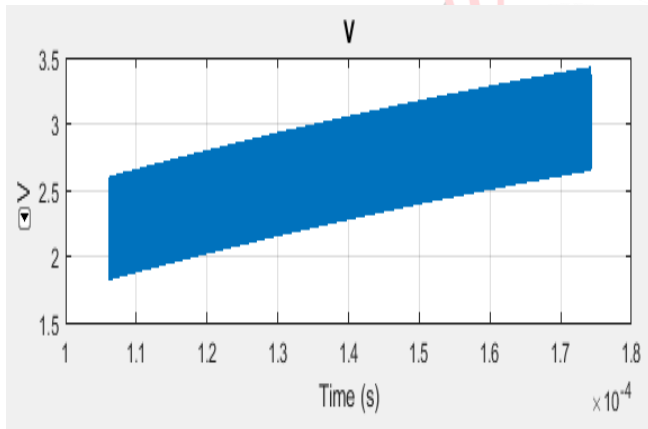**Figure 12. VCO output when voltage request is 4.2v.**

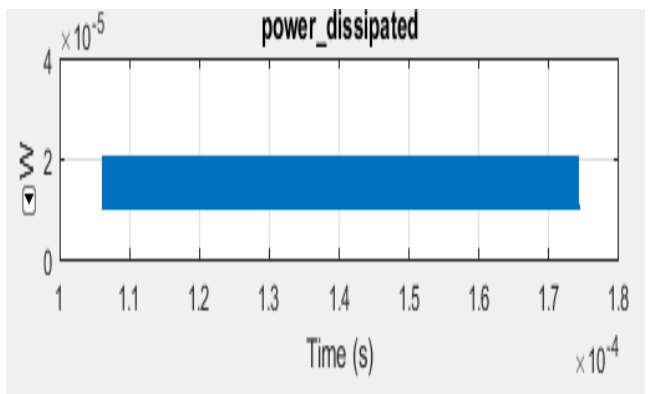**Figure 13. VTD output when voltage request is 4.2v.**

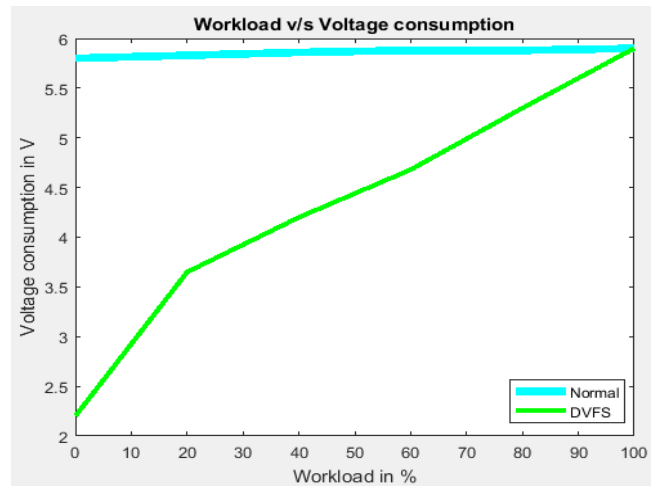**Figure 14. Power dissipated when voltage request is 4.2v.**

Figure 15. Workload v/s Voltage consumption

In figure 15, it clearly shows that, the normal method without considering workload the voltage consumption is between 5.5v to 6v. But in DVFS method the voltage consumption is vary with workload, hence the DVFS is the optimal one.

In the figure 16, it clearly shows that the normal type power dissipation is almost constant for all workload, but in DVFS the power dissipation is also vary with workload. Hence in DVFS method power dissipation is less compare to the normal one.
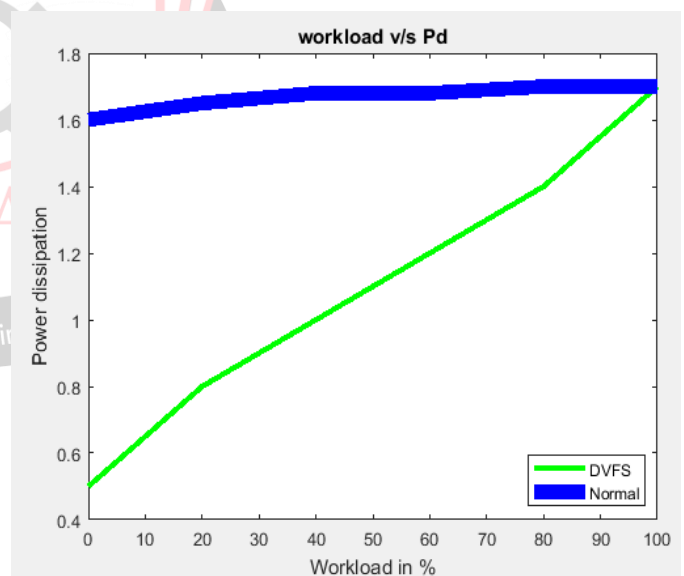

Figure 16. Workload v/s Power dissipation

VI. CONCLUSION

The proposed DVFS technique introduced in this paper, is to vary the supply voltage based on the processor predicted workload. Workload is predicted by processor itself using IPA method. Based on this VCO provides the limited energy. So this significantly improve processor energy efficiency by using optimized supply and reduces power dissipation during run time and required voltage for each workload is different. So it is very useful in battery operated devices and UPS powered devices.

REFERENCES

[1]. Bunescu, Ahmed Louri, "LEAD: Learning-enabled Energy-Aware Dynamic Voltage/frequency scaling in NoCs" 2018

[2]. Mayuri Digalwar, Praveen Gahukar, Sudeept Mohan "Energy Efficient Real Time Scheduling on Multi-core Processor with Voltage Islands" 2018.

[3]. Alankar V. Umdekar, Arijit Nath, Shirshendu Das, Hemangee K. Kapoor, " Dynamic Thermal Management by using Task Migration in Conjunction with Frequency Scaling for Chip Multiprocessors" IIT Guwahati 2018.

[4]. Narender Kumar, Munish Rattan "Implementation of Embedded RISC Processor with Dynamic Power Management for Low-Power Embedded system on SOC" 2015.

[5]. Racho Marinov Ivanov, Lubomir Valeriev Bogdanov "Dynamic Frequency Scaling in Embedded Systems" 2013.

[6]. Philipp Miedl, Xiaoxi He, Matthias Meyer, Davide Basilio Bartolini, Lothar Thiele "Frequency Scaling as a Security Threat on Multicore Systems"2018.

[7]. Sergio Saponara, Luca Fanucci, and Pierangelo Terreni "Architectural-Level Power Optimization of Microcontroller Cores in Embedded Systems"2007.

[8]. Ching-Long Su, Chi-Ying Tsui, Alvin M. Despain "Low Power Architecture Design and Compilation Techniques for High-Performance Processors" 1994.

[9]. O. Ergin, "Circuit Techniques for Power-Aware Microprocessors", Master Thesis, The State University of New York, USA, 2003.

[10]. Lei Yang, Robert P. Dick, Gokhan Memik, "HAPPE: Human and Application-Driven Frequency Scaling for Processor Power Efficiency" 2013.

[11]. C. H. Hsu, "Compiler-Directed Dynamic Voltage and Frequency Scaling for CPU Power and Energy Reduction", Ph. D. Dissertation, the State University of New Jersey, USA, 2003.

[12]. A. P. Chandrakasan, "Low-Power CMOS digital Design, IEEE Journal of Solid-State Circuits", Vol.27, No.4, Pages 473-484, April 1992.

[13]. Diary R. Suleiman, A, Ibrahim, "Dynamic voltage frequency scaling for microprocessor power reduction", 2008.

[14].https//nptel.ac.in/courses/106105034/22