Implementation of Multiplier-Accumulator (MAC) unit using 16-bitVedic Multiplier

Mohammad Nasiruddin, Research Scholar, MIET Gondia, India, mn151819@gmail.com
Dr. Prashant S. Sharma, Supervisor, MIET Gondia, India, pssharma2873@gmail.com
Dr. Vijay S. Chourasia, Co-Supervisor, MIET Gondia, India, chourasiav@gmail.com

Abstract - As the technology is expanding from micro scale to nano scale to deal with nano scale, a new field is developed called quantum computing. Quantum computation based on the principle of reversible operation, in which certain task must be performed in nanoseconds. In order to realize a high-speed multiplier a Vedic algorithm can be applied. The multiplication process involves two steps i.e. formation of partial product and addition of partial product, these two steps are concurrently performed by the Urdhva Tiryakbhyam algorithm of Vedic Mathematics. The Multiplier and Accumulator (MAC) are the vital elements of the digital signal processing. Power dissipation is one of the vital parameter in modern day technology. The objective of a good multiplier is to provide a substantially compact, high speed and low power consuming chip. We have designed a MAC unit which has low power dissipation than the conventional multipliers. In this paper we have compared the results of conventional multiplier with 16-bit Vedic multiplier.

Keywords* —Adder, *MAC, Urdhva Tiryakbhyam Sutra, Vedic Multiplier, Xilinx

I. INTRODUCTION

The appeal for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [1].

With the rapid recent advancements in multimedia and communication systems, the demand of real-time signal processors which can processes audio signals, video/image signals, or large-capacity data processing are increasing day by day. The multiplier-accumulator (MAC) is the necessary component of the digital signal processing such as filtering, convolution, transformations and Inner products. Power dissipation is one of the most critical parameter in modern day technology. The purpose of a good multiplier is to provide a physically compact, high speed and low power consuming chip.

Vedic multiplier is an inspiring solution in today's world for wide range of applications because of its simple architecture and high speed which forms an unmatched combination for doing any complex multiplication computations. The Vedic multiplier requires very less area as compared to other multiplier architecture. Hence the Vedic multiplier is faster than the other multipliers like, booth multiplier, array multiplier and Wallace multiplier. MAC always lies in the critical path that establishes the speed of the overall hardware systems. As MAC has regular and parallel structure it can be realized easily on silicon chip as well. [2]

II. MAC UNIT

In Digital Signal Processing the Multiplier-Accumulator (MAC) operation is the very critical operation not only in DSP applications but it is also critical in multimedia information processing and various other applications. MAC unit consist of multiplier, adder and accumulator. The MAC unit actuates the speed of overall system as it is always lies in the critical path. To establish high speed MAC unit is essential for real time DSP application. In order to improve the speed of the MAC unit, there are two major factors that need to be considered. The first one is the fast multiplication network and the second one is the accumulation. These stages perform the addition of large operands that involve long paths for carry propagation. In recent MAC, accumulation and addition are merging to save the time and power. The MAC unit mostly do the multiplication of two numbers, multiplier and multiplicand, and add this product with result stored in the accumulator. For increasing the speed of MAC unit, fast adder and multiplier circuits are required. Figure 1 shows the basic Structure of MAC unit.

General Architecture of a MAC unit is shown in to the Figure 1. MAC unit contains a multiplier and an accumulator containing the sum of the previous successive products. The MAC inputs are taken from the memory location and then given to the multiplier block. [3]

 DOI : 10.35291/2454-9150.2019.0485

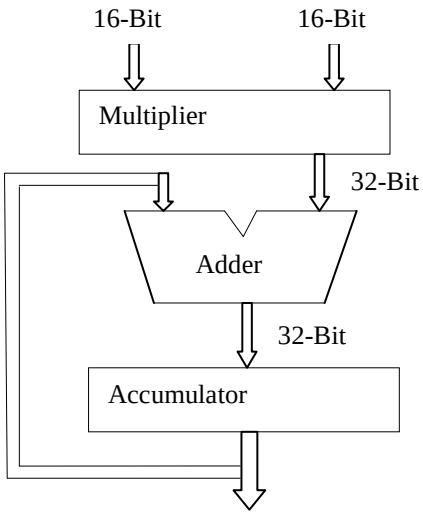

Figure 1 – 32-Bit Final Output unit.

III. PRINCIPLES OF VEDIC MATHEMATICS

The Sanskrit word Veda is derived from the root Vid, meaning of this is to know without limit. The word Veda describes all the Veda-sakhas known to humans. The Veda is a source of all knowledge, incalculable, ever revealing as it is investigated shallower. Swami Bharati Krishna Tirtha who was Sankaracharya of Goverdhan matha puri from 1925-1960, picked a set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda. He established methods and techniques for intensifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics.

These Sutras can apply to every branch of Mathematics and also covers all branches of Mathematics. These sutras can be applied even to the complex problems including a large number of mathematical operations. Application of these Sutras saves a lot of time and effort in solving the complex mathematical problems as compared to the formal methods presently in use. Though the solution of Vedic mathematics seems like magic, the application of the Sutras is perfectly logical and rational. The calculations made on the computers follows, in a way, the principles underlying the Sutras. The Sutras provides methods of calculation as well as it also improves the ways of thinking for their application. [4]

IV. MULTIPLICATION ALGORITHM

Here we have used Urdhva Tiryakbhyam Sutra algorithm for multiplication. The basic steps involved in this algorithm are-

- Take the right hand digit and multiply them together. This will give LSB digit of the answer.
- Multiply LSB digit of the top number by the second bit of the bottom number and the LSB of the bottom number by the second bit of the top number. Once we have those values add them together.
- Multiply the LSB digit of bottom number with the MSB digit of the top one.
- Next step is Similar to the previous step and move one place to the left. Then we will multiply the second digit of one number by the MSB of the other number.
- In the final step simply multiply the LSB of the both number together to get the final product.

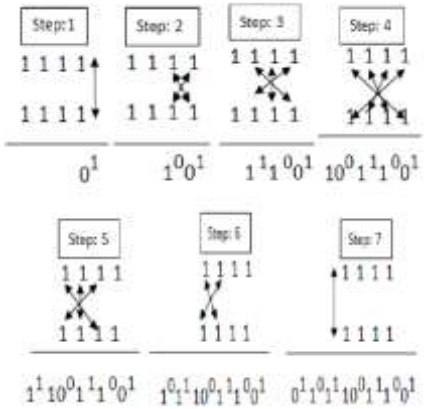

Figure 2-Steps followed in Urdhva Tiryakbhyam Sutra

V. PROPOSED 16X16-BIT VEDIC MULTIPLIER

The 16x16 bit multiplier is made by using 4, 8x8 multiplier blocks. Here the multiplicand are of size (n=16) and the result obtained is of 32 bit. The input is divided into smaller sequence of size n/2=8. These newly formed units are given as input to 8x8 multiplier blocks. Again the new units are broken into even smaller units of size n/4=4 and fed to 4x4 multiply block. The newly formed 4x4 bit unit is again divided in half to get unit of size 2, which is fed to a 2x2 multiply block. The output of 8x8 bit multiplier block, which is of 16 bits data, is sent for addition to an addition tree.

We have implemented the 16-bit Vedic Multiplier and Conventional Multiplier using Xilinx Spartan 3 500E Starter Kit.

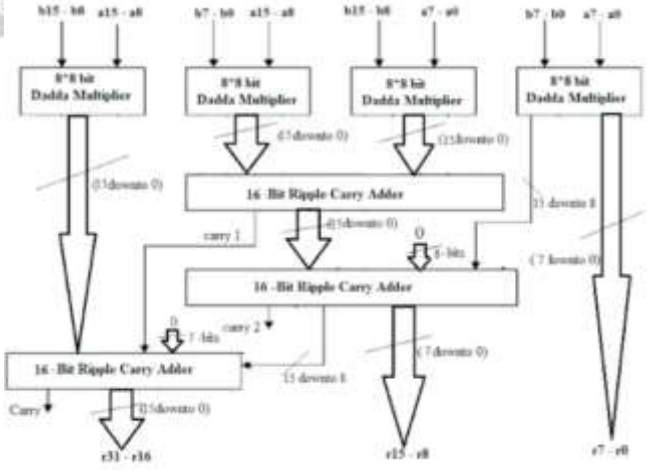

Figure 3 – 16x16 bit Vedic Multiplier

VI. SIMULATION RESULT

A. *Vedic Multiplier*

The results of the 16x16 Vedic multiplier are given in the screenshots below. These results are obtained by using Xilinx Spartan 3 500E starter kit. Figure 3a shows the

 DOI : 10.35291/2454-9150.2019.0485

simulation results of multiplication of two unsigned 16 bit numbers.

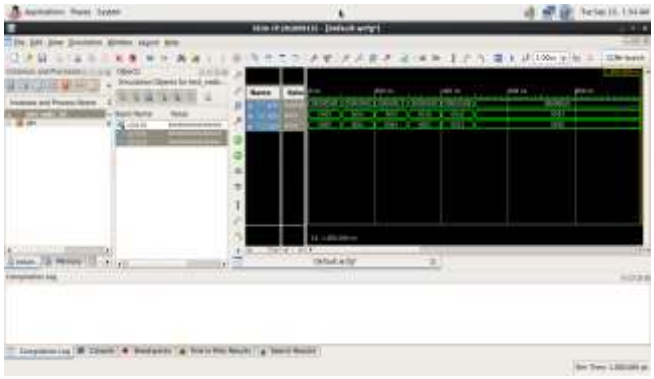

Figure 4a-Simulation output of 16-bit Vedic Multiplier

The 16 bit Vedic multiplier that is built using 8 bit Vedic multipliers. The 8 bit Vedic multipliers are in turn built using 4 bit Vedic multipliers, and the 4 bit Vedic multipliers are built using 2 bit Vedic multipliers, and finally, the 2 bit Vedic multipliers are built using 1 bit Vedic multipliers as building blocks.

Figure 4b shows the device utilization summary when the 16 bit Vedic multiplier is implemented on a Xilinx Spartan 3 500E Starter Kit, and it shows that the 16 bit Vedic multiplier utilizes 502 LUTs and 502 flip flops, as device utilization of FPGAs is expressed in number of LUTs and number of flip-flops utilized.Figure 4c shows that the 16 bit Vedic multiplier is a purely combinational circuit and the maximum combinational path delay from input to output for the given FPGA is 21 ns. Figure 4d shows that the 16 bit Vedic multiplier has an approximate total power dissipation of 106 mW, of which 85 mW is dynamic (switching) power dissipation and 21 mW is static power dissipation.

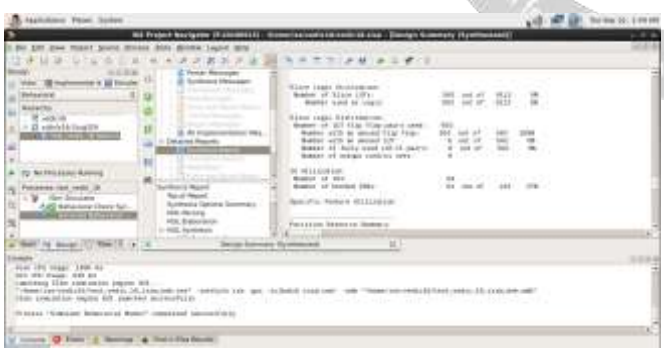

Figure 4b-Device Utilization Summery

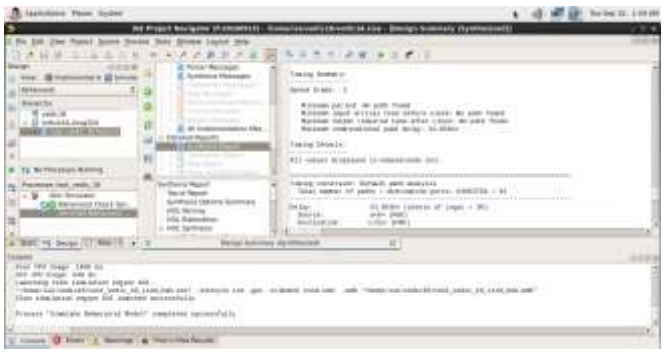

Figure 4c-Timing Report

Figure 34-Power Report

B. Conventional Multiplier

The results of conventional multiplier are given in the screenshots below. This multiplier also realized by using the same software as that of Vedic multiplier.

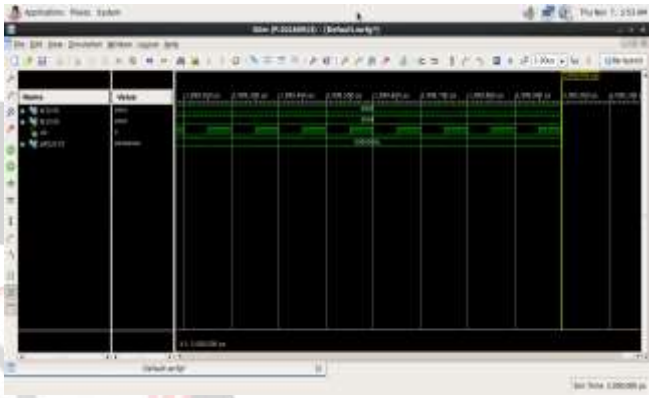

Figure 5a-Simulation output

Figure 5b-Power Report

C. Comparison between Vedic and Conventional Multiplier

Following table shows the comparison between Vedic Multiplier and Conventional Multiplier

Table 1-Comparision

Perticulars	16-bit Vedic Multiplier	Conventional Multiplier
Power	106 mW	198 mW

This comparison clearly shows that there is significant reduction in power dissipation in Vedic Multiplier as compared to Conventional Multiplier.

 DOI : 10.35291/2454-9150.2019.0485

VII. CONCLUSION

In this paper we have compared the conventional multiplier with the Vedic multiplier. The result shows that the Vedic Multiplier is more power efficient in digital plans as compare to conventional multiplier. Table 1 shows the comparison of conventional multiplier and 16-bit Vedic multiplier with Urdhva Tiryakbhyam sutra. It is observed that the Vedic multiplier has 106 mW power dissipation as compared to conventional multiplier which has 198 mW power dissipation. We can conclude that by using Vedic multiplier the power dissipation can be improved. The work can be further extended with the usage of such multiplier along with fully pipelined accumulator in arithmetic logical unit. The Multiplier-Accumulator (MAC) unit can be implemented using fully pipelined accumulator to further increase the speed and reduce the power dissipation.

REFERENCES

[1] Himanshu Thapliyal and Hamid R. Arabnia, "A Time-Area- Power Efficient Multiplier and Square Architecture Based On Ancient Indian Vedic Mathematics", Department of Computer Science, The University of Georgia, 415Graduate Studies Research Center Athens, Georgia 30602-7404, U.S.A.

[2] Muhammad H. Rais, Mohammed H. Al Mijalli, Mohammad Nisar. 2012. FPGA Realization of Braun's Multiplier. Proceedings of *International Multi-Conference of Engineers and Computer Scientists* Vol. I, IMECS 2012, Hong Kong.

[3] P. Jagadeesh, Mr. S. Ravi and Dr. Kittur Harish Mallikarjun, "Design of High Performance 64 bit MAC Unit" *IEEE International conference on Circuits, power and Computing Technologies* [ICCPCT-2013]

[4] C Ranjit Kumar, G Rahul Ram, N Chandu Reddy, "Design of Square and Multiply and Accumulate(MAC) Unit by using Vedic Multiplication Techniques'' *International Journal of Scientific & Engineering Research*, Volume 4, Issue 12, December-2013.

[5] Sumit C. Katkar, Pragati Kene, Shubhangini Ugale, "Design of Efficient 64 bit MAC Unit using Vedic Multiplier for DSP Applications-A Review" *International Journal of Advanced Information and Communication Technology (IJAICT), Volume 1, Issue 9, January 2015*.

[6] S. M. Khairnar, Sheetal Kapade, Naresh Ghorpade 2012 "Vedic mathematics - The cosmic software for implementation of fast algorithms", IJCSA-2012.

[7] Manorajan Pradhan, Rutuparna Panda, Sushant Kumar Sahu 2011, "Speed comparison of 16 X 16 Vedic multipliers", *International journal of computer applications, Vol. 21, No.6, May 2011.*

[8] Aniruddha Kanhe, Shishir Kumar Das, Ankit Kumar Singh, 2012 "Design and implementation of low power multiplier using Vedic multiplication technique", *International Journal of computer science and communication techniques, Vol. 3 No.1 Jan-June 2012, 131-132.*

[9] L. Sriraman, T. N. Prabakar 2012, "Design and Implementation of Two Variable KCM using Multiplier using KCM and Vedic Mathematics ", in *1st International Conference on Recent Advancements in Information Technology, 2012.*

[10] L. Sriraman, T. N. Prabakar 2012, "FPGA implementation of high performance multiplier using squarer", *International Journal of Advanced Computer Engineering & Architecture Vol.2, No.2, June-December 2012.*

[11] Sudhanshu Mishra, Manoranjan Pradhan 2012, "Synthesis comparison of Karatsuba multiplier using polynomial multiplication, Vedic multiplier and classical multiplier", *International journal of computer applications (0975- 8887) Vol. 41 No. 9, March 2012.*

[12] Prashant Nair, Darshan Paranji, S. S. Rathod, "VLSI implementation of matrix diagonal method of binary multiplication", *Proceedings of SPIT-IEEE Colloquium and International Conference, Mumbai, India, Vol. 2, 55*

[13] V. Vamshi Krishna, S. Naveen Kumar 2012, "High Speed, Power and Area efficient Algorithms for ALU using Vedic Mathematics" *International Journal of Scientific and Research Publications, Volume 2, Issue 7, July 2012.*

 DOI : 10.35291/2454-9150.2019.0485