To Design 12-Bit Low Power and Low Voltage Segmented Successive Approximation Register Analog-to-Digital Converter on 45nm CMOS Technology

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Abstract: Successive approximation resister (SAR) is an Analog-to-Digital Converter which accomplishes low power utilization because of its simple and easy design. SAR ADC does not required an operational amplifier, so they are invaluable in CMOS scaling technologies. The design is specially used for battery controlled or versatile applications which required medium resolution, medium speed and require low-power consumption and small form factor. In this paper the design of 12 bit SAR ADC working at 50MHz frequency and supply voltage at 0.3V in 45nm CMOS Technology. The power utilization of 0.005nW is accomplished. The ADC utilizes a segmented capacitive DAC array, Dual tail comparator, and SAR circuit containing D-flip-flops. In research the dynamic comparator expend lower control when contrasted with different methodologies. Along with these, different models of the dual tail comparator are proposed and compared with respect to the power used, speed and accuracy. Subsequently, the dual rail comparator is chosen to be utilized in the designed ADC.

Keywords — Successive approximation resister, Analog-to-Digital Converter, Dual tail comparator, Segmented capacitive DAC array.

I. INTRODUCTION

According to the strict requirement of the current networking technology on power consumption, a low power successive approximation registers Analog-to-Digital Convert circuit depends on segmented capacitor has been designed. An essential challenge is a simple structure lies in accomplishing the best balance between four principal measurements for example Voltage, Current, Power proficiency and die size or area. The idea of this trade-off is connected to basic qualities of transistors and is profoundly reliant on technology scaling.

Successive Approximation Resister (SAR) Analog-to-Digital Converter (ADC) accomplices low power utilization because of its basic design dependent on the overwhelming advanced substance. SAR-ADC does not require an additional operational amplifier, so they are beneficial to CMOS innovation scaling. The primary confinement of SAR-ADC is a low rate sampling, which connected to its serial decision making nature. SAR ADC is the best decision for portable battery powered applications and need just average resolution (8-12 bits) and medium speed (10-100 Mega-Sample/Sec). However it requires less power utilization. The architecture is generally utilized in low vitality radios like Bluetooth for Body-region systems, in independent convenient sensor frameworks, in numerous biomedical applications like ECG monitoring and many more. Various advanced procedure and structure strategies used for improved performance is proposed persistently. It incorporates asynchronous operation, charge sharing technique, capacitor splitting technique, etc. This work centered on the investigation of the segmented operation of SAR logic. It probably investigated the most recent trend of ADC's main analog components like Comparators and the DAC. All through the work, the design trade-off is constantly remembered. However the power is under the fundamental objective, different measurements may not be yielded to a huge degree, breaking the practical balance and in general structure of the architecture.

II. RELATED WORK

The work proposed by Rikam et. al [1] is the design of 11-Bits 40KS/s Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) structure for sensor applications the capacitive DAC array which reduces the power consumption and also improved the linearity by advanced design. This result in 67.27-dB SNDR and 83.7dB SFDR at 40KS/s under a 1.8V supply in another research author Wang et.al [2] proposed a method to increase the speed of conversion of one bit digital code 4-times faster than conventional structure. The parallel capacitor array is utilized to lessen the kickback noise effect brought about by the DAC cluster. A 10-bit 150MS/s SAR-ADC is actualized on 65nm CMOS technology. The structure achieves SFDR of 83.77dB with ENOB 1.47mW power utilization at a 1.2V supply. Also worth to mention

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the work carried out by Roy et al. [3] proposed the idea of SAR which applies a flash component is proposed which divide the dynamic range into 2N segments. The flash enhances the sampling rate which also improves the Figure of Merit. The idea implemented on 180nm CMOS technology. The proposed design produces a Signal-to-Noise-and-Distortion Ratio (SNDR) of 32.42 dB and 38.07 dB. Chahardori et al. [4] proposed the idea of a low power 4-bit 1.6 GS/s flash ADC which used semi-pipeline chain to improve the power consumption by 20% compared to the conventional structure. The converter uses 15.5 mW from a 1.8V supply, yielding a Figure-of-Merit of 695 fJ/ transformation. The design carried out on 0.18µm standard CMOS process. The segmented architecture for SAR-ADC design is proposed by Saberi et al. [5] improves the power consumption and static linearity performance. The entire DAC and the digital circuit consume 30% less power than the traditional plan. The standard deviation of the differential nonlinearity is decreased by factor of $2\sqrt{2}$. Author Wu et al. [6] design a pipelined SAR ADC with loading free architecture. In this author merge the feedback capacitor and the array of the capacitor of the second stage to reduce the op-amp output. This results in reduction of power and tolerates non-idealities in the main stage. The design implemented on 90nm CMOS process which involves functioning area of 0.117mm^2. The research carried out by author Mao et al. [7] the idea is proposed for biomedical application in which hybrid switching plan is proposed to reduce the all capacitor count. The architecture designed in 130nm CMOS process with the area of 0.16mm^2. The designed consumed 110nW at 1.0V power supply. Ting et al. [8] planned a segmented resistor-string DAC based ADC. The capacitive stacking reduces to upgrade the speed DAC. Area of the structure is additionally decreased by the parallel associated substrings. The author Maddox et al. [9] presents the charge sharing SAR-ADC which valuable for the poor linearity because of the unregulated reference voltage during bit exchange. The ADC designed on 90nm 1P9M CMOS technology and consumes 2.72 mW at 1MHz. Sauerbrey et al. [10] proposed an ADC working at ultra supply voltage. The circuit implemented on 0.18µm standard CMOS technology. The use of sample and hold circuit and Capacitive DAC array keep away from the utilization of operation amplifier. The ADC has a signal to noise and distortion ratio of 51.2 and 43.3dB for supply voltages of 1.0 and 0.5V.

III. METHODOLGY

The proposed project consist of designing and execution of a low power low voltage 12-bit segmented SAR-ADC on 45nm CMOS Technology with the main application of enhancing the speed of conversion and tumbling the overall power use of the circuit. The main components of ADC are Comparator and DAC. The Figure 1 illustrates the proposed method for segmented SAR ADC. The analog input of the infinite signal is given to the Sample-and-Hold (S&H) circuit. The Sample-and-Hold circuit samples each bit at a time. The samples will be held till the processor gets ready.

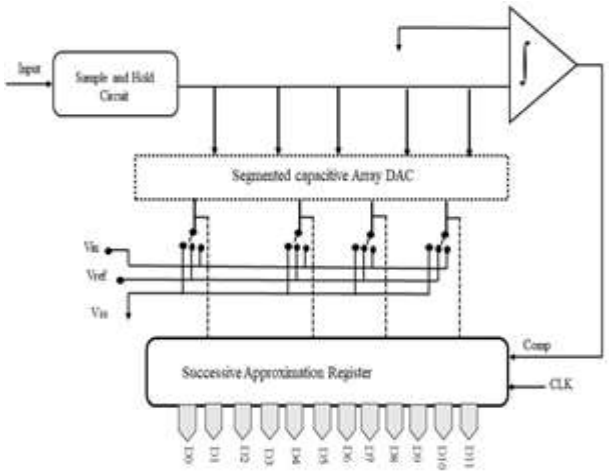

Figure 1 Schematic of Segmented SAR-ADC

The output of the Sample-and –Hold circuit is given to the capacitive array which is used for the charging and discharging of the current in the circuit. The capacitor array is connected to the bottom plate. It is used for discharging the capacitor through the specific path and the bottom plate act as a switch between capacitive array and the discharging path of the capacitor in the circuit. The output of the capacitive array is given to the comparator. The comparator compares the output of the capacitive array with the Vin voltage and the output is given to the input of the Digital-to-Analog Converter (ADC). If the input of capacitive array is greater than Vin (+) voltage then the output will be Vcomp (+) or if the input of capacitive array is less than Vin(-) voltage then the output will be Vcomp (-). The output of SAR is converted to analog output by the DAC and this analog output is compared with the input analog sampled value in the comparator. The operational-amplifier gives a high or low clock pulse rate depends on the difference between the logic circuit.

A. Segmented Capacitive DAC Array

According to the present research, the technical problem which is produced by the segmented DAC and the capacitor array is major. To solve this major problem some parameter needs to fix like parasitic capacitance between the sub-arrays, eliminating the gain errors, improving the linearity and the INL/DNL characteristics. The advantage of binary-weighted DAC is its simple design as no decoding logic is require. However, there are some drawbacks also. These drawbacks were connected with real bit transition at the mid-code transition, the most vital capacitor values. It was hard to accomplish and such matching would never be ensured. In addition, the blunder brought by the dynamic behavior of the switches brings glitches in the output signal. Such glitches contain an enormous non-linear signal component, apart from output signal, it will spurs in the frequency domain. In order to solve the above drawbacks,

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and segmented SAR-ADC is design in which the 4 MSB bits are decided by the thermometer codes and 7 LSB bits decided by the binary code. In sampling cycle, the input is sample at the top plate of the capacitors.

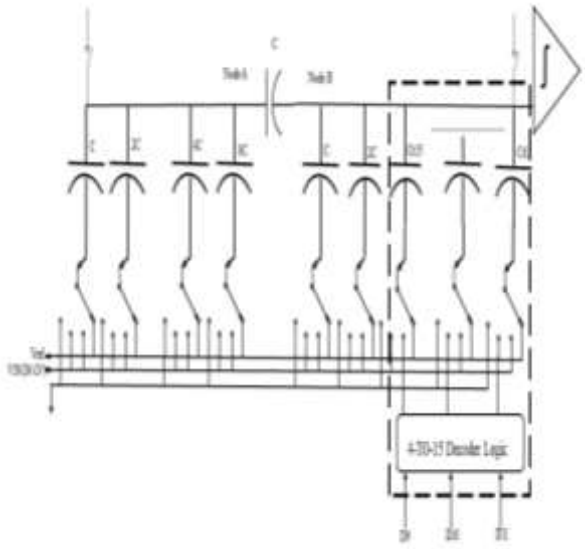

Figure 2. Segmented capacitive DAC array

The first comparison is done at the end of the holding cycle. There are two cases for the first comparison. If the first comparison is low sequence then it will continue to switch capacitors from Vref. The Figure 2 shows a segmented capacitor array with 4-bit thermometer coded DAC to improve the linearity operation.

As seen in Figure 2 the 4-MSB bits on the capacitor array was made by the thermometer code. The 12-bit DAC is designed with the segmented unit bridge capacitor to help in decrease the size and area of the capacitors require. In the end, to limit the current require is to restore the capacitor array. Combination of the sub-DAC array and thermometer code is utilized to improve the linearity of the circuit. The array capacitor of a segmented DAC is design according to the present research. A comparator is consisting of at least two subs–array and at least one bridging capacitance. The positive input of the comparator is connected to the common node of the capacitor sub array and the negative input terminal connected to a reference voltage signal. An output signal terminal should be connected to the entire capacitor sub-arrays control switch. Each bridge capacitor is connected with two weighted capacitor sub-array of adjacent quantization bits. The lower sub-array capacitor of each bridge capacitor is connected in parallel to the variable capacitance and compensation capacitor.

B. Dynamic Dual-Tail Comparator

The Double-tail comparator has two different paths for discharging the current. This structure also has less stacking of transistors when appeared in common comparator. The advantage of binary-weighted DAC is its simple design and function because no decoder is required yet some drawbacks are present. These drawbacks are connected with significant major bits transitions.

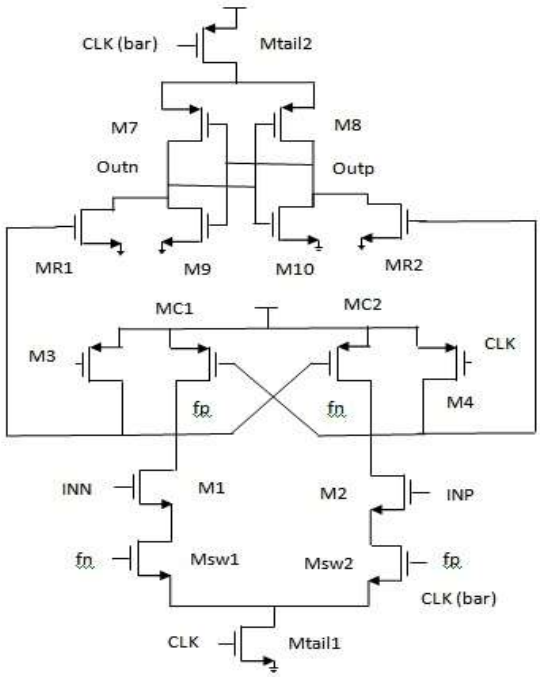

Figure 3. Dynamic Dual-tail Comparator

At the mid-code transistor, the most significant capacitor value should be coordinate to the total of the various capacitor values below the 0.5 LSB's. Due to measurable extend, it is hard to achieve and such coordination would never be ensured. Furthermore, the errors due to the dynamic behavior of the switches bring glitches in the output signal. Such glitches contain especially nonlinear signal parts, even some minor part of the output signal and it will shows itself as a spurs in the frequency domain.

IV. RESULT AND DISCUSSION

The implemented ADC architecture shows in Figure 5. Is design in Tanner EDA software The control circuitry and the timing signals required for the proper functioning of the circuit are also presented.

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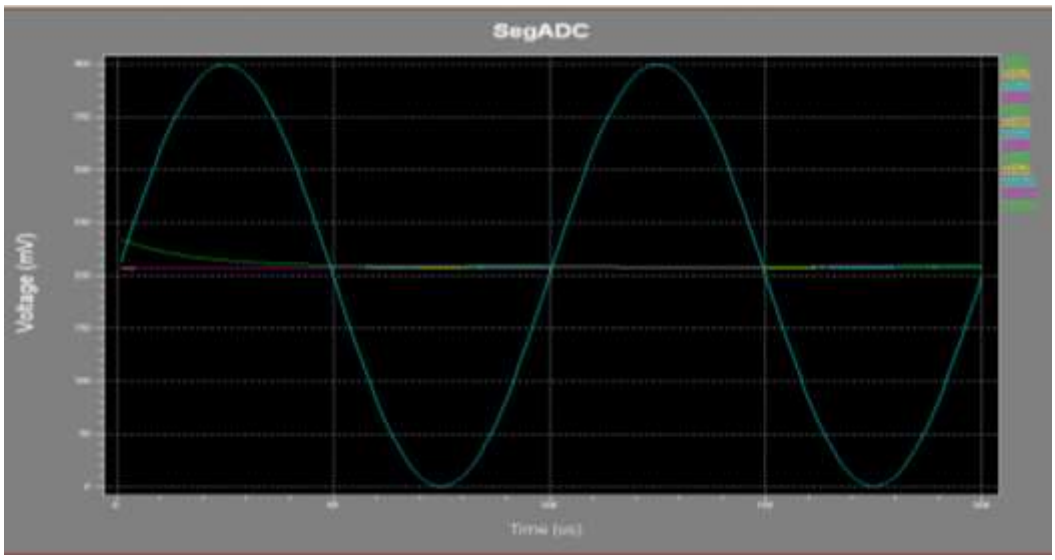

Figure 4. Waveform of implemented SAR ADC

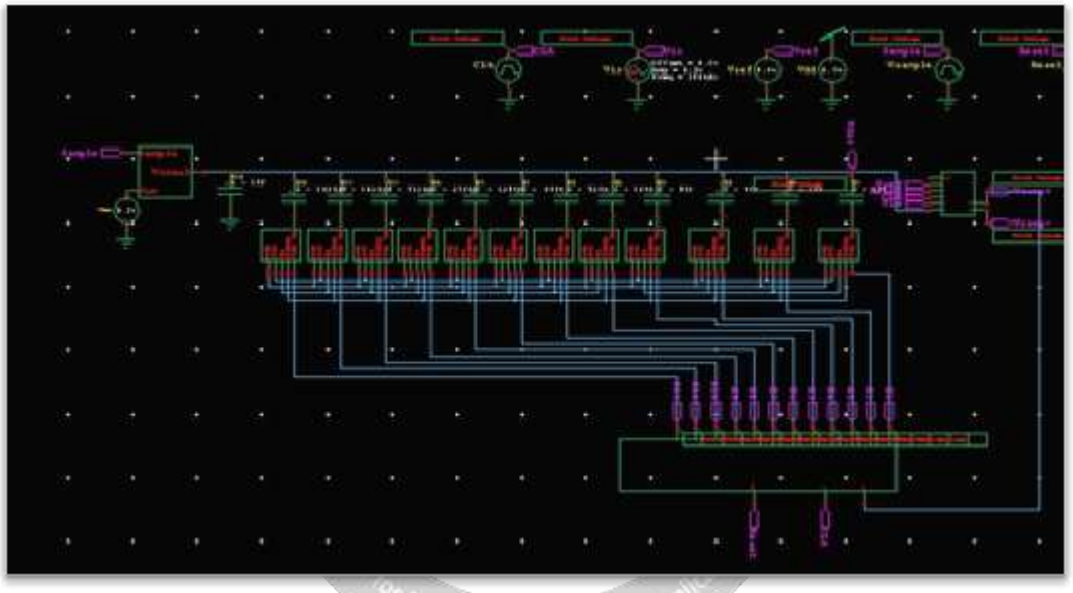

Figure 5. Implementation of proposed SAR-ADC

Parameters	Paper I	Paper II	Paper III	Paper IV	Paper V	Paper VI	Paper VII	Paper VIII	Paper IX	Paper X	Paper XI	This work
BITS	11bits	10bits	7bits	4bits	10bits	12bits	12bits	-	16bits	-	4bits	**12bits**
CMOS TECHNOLOGY	0.18 µm	65 nm	180 nm	0.18 µm	-	90 nm	130 nm	0.18 µm	55 nm	0.18 µm	0.18 µm	**45 nm**
CURRENT	1.0µA	-	-	-	-	-	-	-	-	-	-	**0.018 nA**
VOLTAGR APPLY	1.8V	1.2V	-	-	1.0V	-	1.0V	-	-	1.0V	1.8V	**0.3V**
POWER CONSUMPTION	-	1.476 mW	-	15.5 mW	-	2.72 mW	110 nW	339 µW	6.95 mW	30 µW	10.6m W	**0.005 nW**
INL	-0.76 /0.72 LSB	-	-	0.3 LSB	-	-	-	±1.00	±0.8 LSB	-	<0.08 LSB	**<0.33 LSB**
DNL	0.49/0 .48 LSB	-	-	-	2⁻²	-	-	±0.60	±0.3 LSB	-	<0.18 LSB	**<0.44 LSB**

Table I: Comparison with other published work

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The simulated time could be decreased from several minutes to a couple of seconds by replacing the component. In order to increase to conversion speed, dual tail comparator was used which consumed less power than conventional comparators. Approaches closer to reducing the impacts of the capacitor mismatch were utilizing some type of adjustment or digital error correction. Rather than the source of distortion, the power uses by DAC was approximately equally divided. This implies a large reduction of power was hard since a few pieces of the structure must be improved.

The pre-requisites on the reference voltage were severe as a result of the huge capacitance DAC array that must be charged. Segmented DAC array architecture requested contrast with the capacitive array. Simulation shows that the sampling frequency could be expanded to around 500MS/sec, which is an indication of a dependable design. The ADC to work with DAC must be quick enough to settle before the comparator decision. Since the time designated for every bit is relies on the sampling.

Finally, both existing design and proposed design was simulated using Tanner EDA software in 90 and 45nm CMOS Technology. Their result is compares and values were tabulated below on Table II.

Table II: Different blocks of SAR-ADC's power consumption

BLOCK	POWER CONSUMPTION AT 90NM CMOS TECHNOLOGY	POWER CONSUMPTION AT 45NM CMOS TECHNOLOGY
VOLTAGE SUPPLY	0.5 V	0.3 V
DAC	191.02 µW	1.09 µW
SAR	26.14 µW	41.6NW
COMPARATOR	15.42NW	2.75NW
TOTAL CURRENT	2.14MW	18.61 µW
TOTAL POWER	1.39MW	5.56 µW

V. CONCLUSION

This research introduces the execution of 12-bit SAR-ADC working at 50MHz frequency and supply voltage 0.3V in 45nm CMOS Technology. The power utilization of 0.005nW

was accomplished. The ADC utilizes a split/segmented capacitive array DAC, dual-tail comparator, and a SAR controlled logic containing simple D flip-flop. In this work, after studying the different possible structure of SAR logic, they were implemented and compared in terms of power consumption and CMOS Technology. Comparison result obtained indicates that the designed conventional SAR logic with a D flip-flop consumed the lowest power 0.005nW at 45nm CMOS Technology. In this way, the power utilization of the SAR controlled circuit was overall decreased and used just half of the absolute power. Designing the comparator was a crucial part of ADC design. In this work, comparator performs an important part. The different kinds of comparators were examined, such as open-circuit comparator, pre-amplifier preceding a latch comparator, and dynamic comparators consumes low power with different methodologies. Various design of double rail-tail comparator were executed and compared with power, rail, accuracy, and die size. Therefore, the dynamic double tail comparator was chosen to design the ADC.

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