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Review paper on Convolutional encoder for different code rate based on FPGA

[1]S.D.Giri, [2]P.P.Patil, [3]A.R.Salunke

[1,2,3]*Dept. of Electronics & Telecommunication, JNEC,* Aurangabad, INDIA.

[1]sunitagiri@jnec.ac.in, [2]patil.pratibha91@gmail.com, [3]aartisalunke@jnec.ac.in

Abstract- In this paper, in OFDM baseband processing systems a modified FPGA schemes using Vivado2016.1 for the Convolutional encoder is presented. The proposed design shows Convolutional encoder for different rate. The Convolutional encoder is finite state machine which contain a memory of past inputs and also a finite number of different states. Convolutional codes as well as other codes are used for correct bit errors at the receiver, are called Forward Error Correction (FEC). FEC schemes are an essential component of wireless communication systems (such as 802.11).

Keywords- Convolutional encoder, data rates, FPGA, VHDL, Vivado 2016.1.

I. INTRODUCTION

Coding is a technique where redundancy is added to original bit sequence to increase the reliability of the communication. There are many types of coding techniques used to correct different error. Convolutional encoding method using Vivado 2016.1, a good technique used for correcting errors that occur during data transmission. Convolution code is one of the most important for error controlling performance. Convolutional encoder outputs are associated with the encoded elements at present and also affected by past elements. These codes plays a role in low-latency applications such as speech transmission.(Yan Sun1, Zhizhong Ding2,2012)[1],(A.Msir,F. Monteiro,2004), (Zafar Iqbal, Saeid Nooshabadi, Heung-No Lee,2012) [2]Convolutional codes are defined by following parameters; (*n*,*k*,*m*,*L*).

n = number of output bits
k = number of input bits
m = number of memory registers
L = constraint length[2]

Code Rate is the ratio of number of input bits to the number of output bits (k/n). Constant length is the number of delay elements in the Convolutional coding[3]. For example, L= 3, there are two delaying elements. Where, n>k. The quantity *k/n* is called as code rate and it is a measure of the efficiency of the code. Commonly *k* and *n* parameters ranging from 1 to 8, *m* from 2 to 10 and the code rate from 1/8 to 7/8 except for deep space.

Constraint Length, L = *k (m*-1*)*

The constraint length L represents the number of bits in the encoder memory that affect the generation of the *n* output bits. The constraint length L is also referred to by the capital letter K.

II. METHOD

In Convolutional Encoder shifting is done by using shift registers. Delays can also be used in place of shift registers. Result outs as coded bit stream. Figure 1 shows the block schematic of a generalized Convolutional encoder. The structure of Convolutional code is simple. There are m memory register and n mod-2 adder to represent the n output bits.[4]

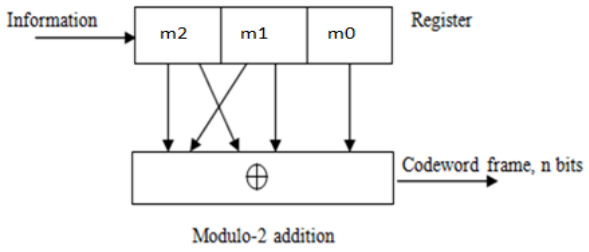

Figure 1: Basic Convolutional encoder

A. Rate 1/2

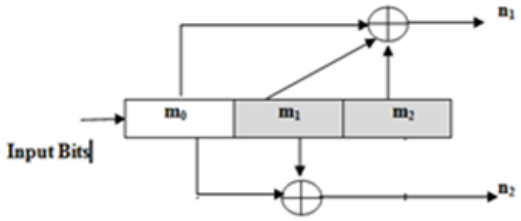

Figure 2: 1/2 Code rate Encoder

If initially Input=0 and m0=0, m1=0, m2=0

So, Output=00

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Input=1, 1is shifted to m0

m0=1, m1=0, m2=0

Thus, Output=11 and so on.

B. Rate 1/3

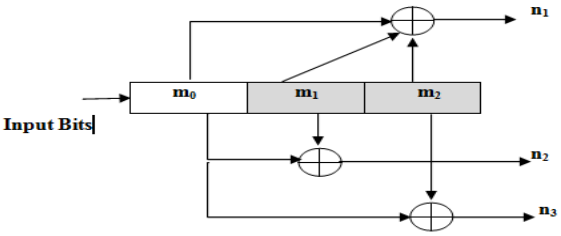

Figure 3: 1/3 Code rate Encoder

If initially Input=0 and m0=0, m1=0, m2=0
So, Output=000
Input=1, 1is shifted to m0
m0=1, m1=0, m2=0
Thus, Output=111 and so on.

C. Rate 2/3

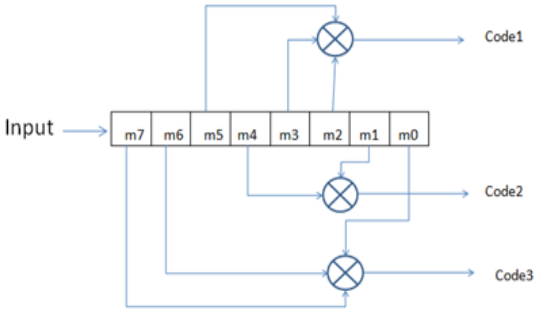

Figure 4: 2/3 Code rate Encoder

From Fig.4, If Input=00
Then, m7=0, m6=0, m5=0, m4=0, m3=0, m2=0, m1=0, m0=0
Output=000
Input=10
Then, m7=1, m6=0, m5=0, m4=0, m3=0, m2=0, m1=0, m0=0
Output=001 and So on.

III. Workflow For Different Code Rate

A. Convolutional encoder of Rate ½

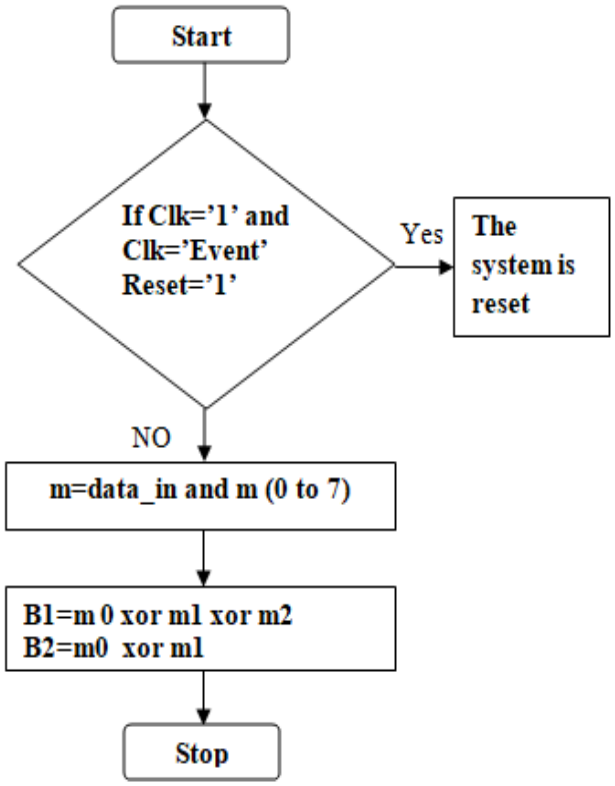

Figure 5: Rate 1/2 convolution encoder

B. Convolutional encoder of Rate 1/3

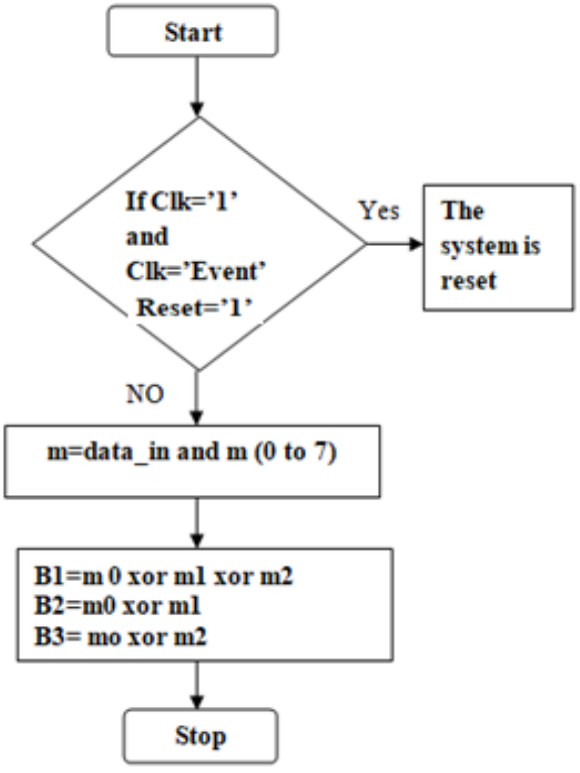

Figure 6: Rate 1/3 convolution encoder

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C. CONVOLUTIONAL ENCODER OF RATE 2/3

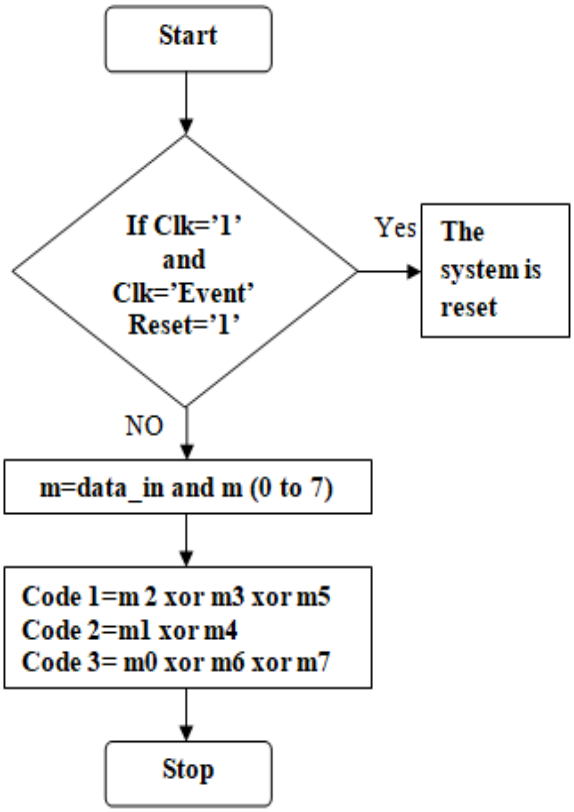

Figure.7: Rate 2/3 convolution encoder

If 2-bit input is applied to encoder, it generates 3-bits as output according to given polynomial. Encoder consists of 1-bit Shift Registers and XOR gates.
Above workflow describes the design of Convolutional encoder. It shows conditions to perform designing.

IV. RESULTS AND RTL SCHEMATICS

A. Rate ½

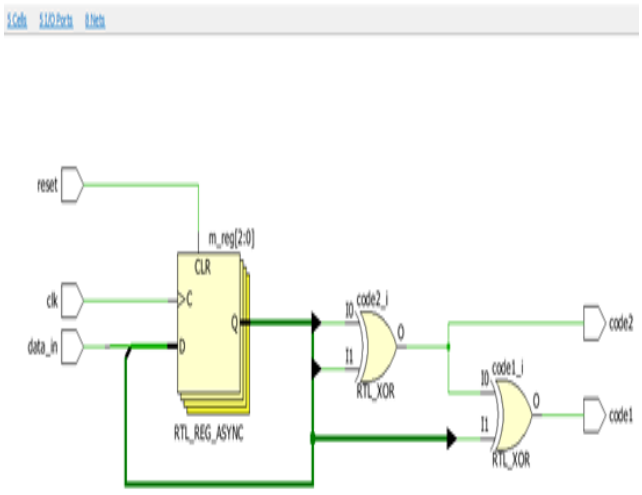

Figure.8 :(i) RTL Schematic for ½

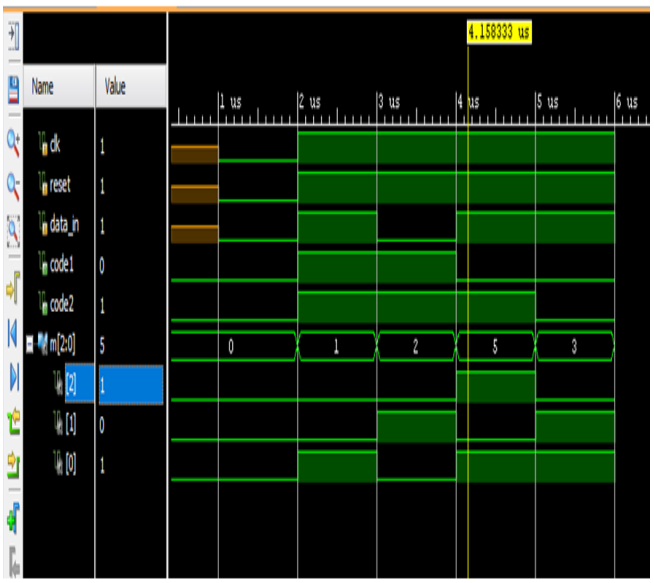

Figure.8: (ii) Result waveform for Rate ½

Fig (8-i) shows RTL Schematic for the rate 1/2 and Fig. (8-ii) shows waveform for rate ½ Convolutional encoder
In above waveform of encoder here Clock is used for Synchronization. Reset is used for Initializing all the blocks. All inputs to the block are synchronized at rising edge of the clock. At every rising edge of clock pulse the system accepts new value of data and processes according to algorithm implemented and produces the output at next rising edge of clock. In the waveform initially code1 and Code2 is 0. Code1 is 1 for 2 to 4 µs and code2 is 1 for 2 to 5 µs and it again becomes 0 .
The output is converted into
O- 0(00)
I -3(11).

B. Rate 1/3

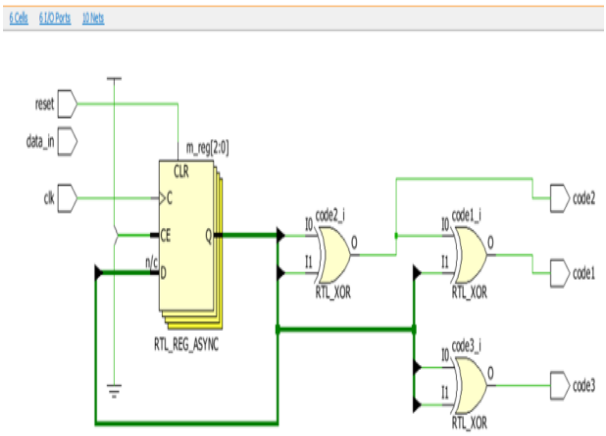

Figure 9: (i) RTL Schematic for 1/3

Figure 9: For data rate 1/3 (i) RTL Schematic (ii) Result shows waveform for rate 1/3 Convolutional encoder The output is converted into

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O- 0(000)
I -7(111)

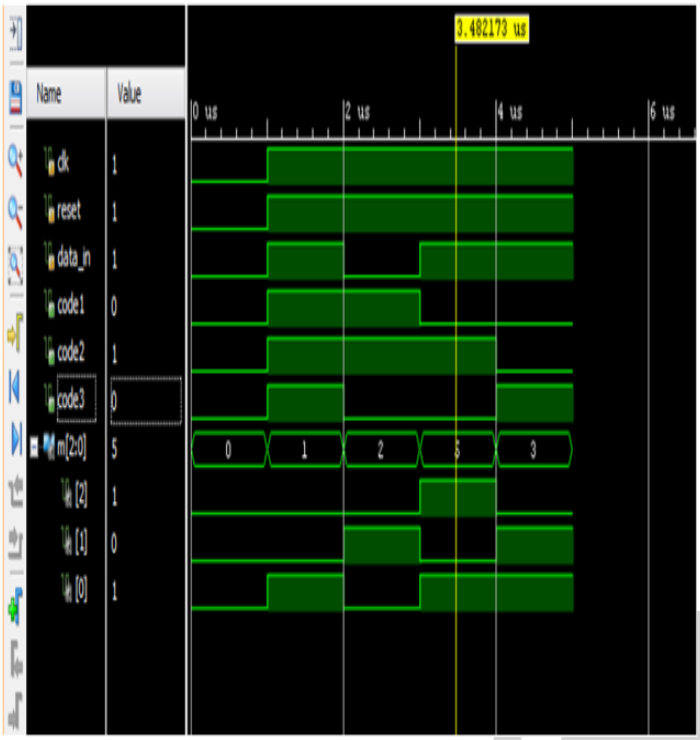

Figure 9 :(ii) Result waveform for Rate 1/3

C. Rate 2/3

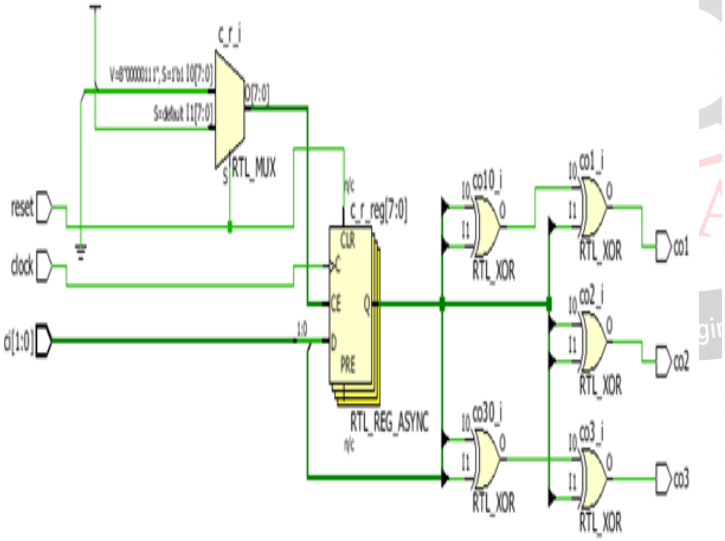

Figure10 :(i) RTL Schematic for Encoder 2/3

Figure10: (ii) Result waveform for Rate2/3

Figure10: For data rate 2/3 (i) RTL Schematic (ii) Result waveform. The output is converted into
O0- 0(000)
10 -1(001)

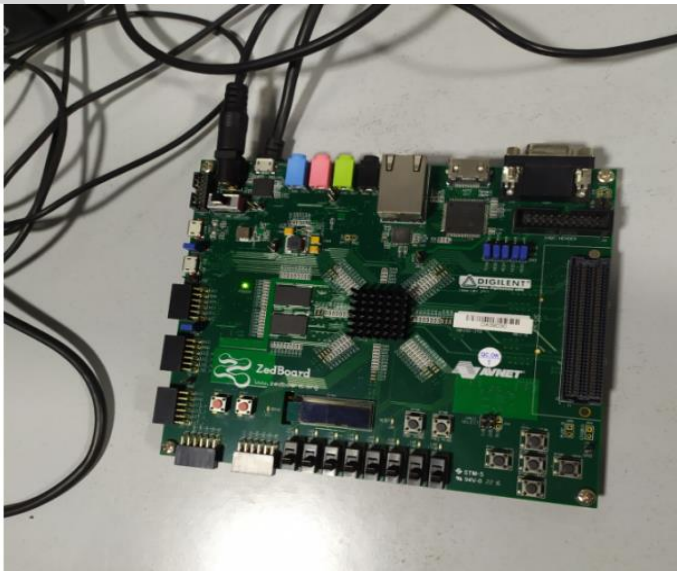

Figure 11: FGPA Implementation

V. CONCLUSIONS

This paper presents design of the structure of Convolutional code to reduce the influence from multi path and channel noise. Such a system can achieve flexibility with regard to changing data rates, increasing range, and increasing diversity, while offering efficient resource utilization.

This design is capable of transmitting data, in air errors and noise are tried to be minimized by using channel coding technique. The use of error-correcting codes has proven to be an effective way to overcome data corruption in digital communication channels. The data speed can be increased by using different combinations of encoding and modulation techniques.

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