Self Organizing Map Based Vector Quantizer for Lossy Image Compression

[1]Mr.Dinesh S,[2]Ms.Saranya K,[3]Rajadurgamani R, [4]Kowsalyadevi G, [5]Vinitha A

[1,2]Assistant Professor,[3,4,5]UG scholor, Department of Electrical & Electronics Engineering

Dr. Mahalingam College of Engineering and Technology, Coimbatore,India.

[1]sridinesh21@gmail.com, [2]saranya@drmcet.ac.in, [3]rajadurgamani@gmail.com,

[4]kowsiguna16@gmail.com, [5]vinithaanbalagan30@gmail.com

Abstract - In this paper image compression is performed based on vector quantization(VQ) technique by using Linde-Buzo-Gray algorithm. A vector quantizer based on self organizing map(SOM) is implemented to obtain a optimized values of area, power and delay. The blocks designed using the verilog program involves squared difference unit block, arithmetic block, minimum distance search circuit. The ASIC parameters such as power, area and delay of each block are calculated using Cadence-EDA tool.

Keywords - Cost efficiency, Image Compression, Vector Quantization

I. INTRODUCTION

In images it carries redundant, irrelevant and useful information. Redundant information is the deterministic part of the information, which can be reproduced without loss from other information contained in the image. Irrelevant information is the part of information that has enormous details, which are beyond the limit of perceptual significance. Useful information, on the other hand, is the part of information, which is neither redundant nor irrelevant. Lossy compression removes some data from the original file and saves the image with a reduced file size. The data to be disregarded can be set by setting the image compression rate. The primary goal of data compression is to develop techniques of coding information sources such as speech, image and video to reduce the number of bits required to represent a source without significantly degrading its quality. It is to represent an image in the fewest number of bits without losing the essential information content within**.**

II. VECTOR QUANTIZATION

Vector quantization (VQ) is a lossy digital compression technique. In Vector quantization based compression algorithms the amount of stored and transmitted data can be reduced with a readily adjusted trade-off between compression ratio and implementation size. These features are important in multimedia processing and communications, etc. In VQ loss in the original information must be kept as low as possible and it can be reduced by simply using a larger suitably-designed codebook. The resulting extra search time can be minimized by using parallel computational elements. VQ is applicable for single dimensional and three dimensional spaces. It reduces the memory occupied and thus known as compression. For example, if an 8 – bit data is taken as input, it can be stored in 3 bits. During VQ , the numbers 0 to 1.9 are commonly represented as 1 and 2 to 3.9 are commonly represented as 3 and 4 to 5.9 are commonly represented as 5 and so on. Hence, after VQ, an 8 – bit number can be stored in 2 bits but the original number is not retrieved as such.

The source data is partitioned into equal-length vectors. Each vector is then replaced with the index of the closest matching code vector that is contained in a given codebook by encoding process. The indexes are then converted back to the corresponding code vectors during decompression in the decoding process. The principle of generating a codebook of a given size is to minimize the expected error distances to the input vectors over the expected input data domain. The size of the codebook (i.e., number of code vectors) determines the trade-off between the accuracy of the coded representation and the transmission bit rate of code vector indexes. In 1980's, Linde Buzo Gray (LBG) proposed a VQ codebook generation algorithm. A training sequence is used to generate an efficient codebook, and that codebook is then used to encode subsequent source or input vectors. The use of a training sequence makes it possible to generate a codebook with reduced computational cost. Although other efficient codebook generation approaches have been developed, the LBG algorithm was selected to generate our codebooks because of its reported efficiency.

 DOI : 10.35291/2454-9150.2020.0159

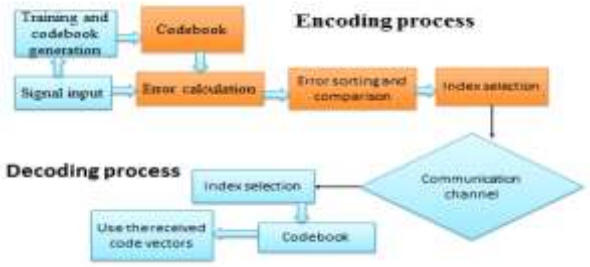

Fig .1: Block diagram for the encoding and decoding process in Vector Quantization.

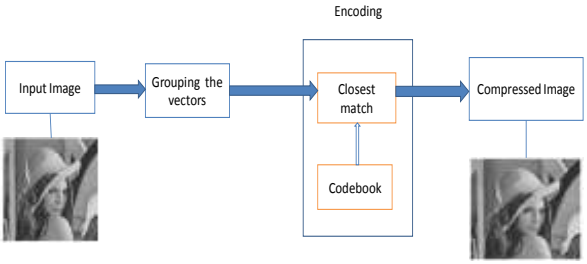

Fig.2: Block Diagram of LBG Algorithm

III.LINDE-BUZO-GRAY ALGORITHM

LBG algorithm is like a K- means clustering algorithm which takes a set of input vectors as input and generates a subset of vectors as output according to similarity measures. Image is divided into blocks, so that each block appears as d-dimensional vector. Initial codebook is chosen randomly. The initial chosen codebook is set a centroid and other vectors are grouped according to the nearest distance with the centroid similar to K-means clustering. To get a new codebook find a new centroid of every group iteratively. Repeat the previous process till the convergence of the centroid of every group. Image Compression can also implemented using clustering concept for codebook generation based on modulo operation. In this paper compact vector quantizer based on the self-organizing map is used. In this vector quantizer, we solve the codebook learning mode and the image encoding mode by using a -binary-adder-tree where the arithmetic units are thoroughly reused.

IV. SELF ORGANIZING MAP

Self Organizing Map gives a data visualization technique which aids in reducing the dimensions of data to a map helps in understanding high dimensional data. SOM also represents the concept of clustering by grouping similar data together. Hence it can be said that SOM reduces dimensions of data and display the similarities among data. It can compress the information of input data while processing. It is usually constructed by components named neurons which are arranged in the form of regular grid of two dimensions. Each neuron contain weight vector, W_i and one d-dimension vector.

$$W_i = \{w_{i1}, w_{i2}, \ldots\ldots w_{id}\}$$

Based on the criterion of similarity matching between input vector and weight vectors neurons are adopted to input vector during the learning step.

$$X = \{x_1, x_2, \ldots\ldots x_d\} \in R^d$$

Winner neuron is regarded as the neuron whose weight vector is the closes to one to the input vector.

Squared Difference Unit block consists of sixteen bit subtractor, multiplexer, D-flipflop and multiplier. Multiplexer controlled by an independent signal s1, which is selection line of a multiplexer. By changing the value of s1, SDU can output either $(x_j\text{-}w_{ij})^2$ or $\propto(x_j\text{-}w_{ij})$ these are the basic elements for calculating Squared Euclidean Distance(SED), (D^2_E). Input vector and weight vector is given to the subtractor as input. The output of the subtractor is given to D-flipflop and multiplexer for multiplier output from the mux and D-flipflop is given as input and the output is fed to RCBAT block.

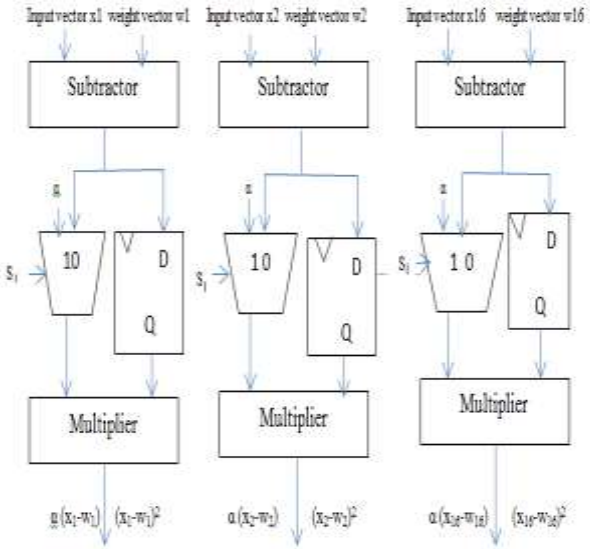

Fig.3: Block diagram of squared difference unit

Reconfigurable Complete Binary Adder Tree block consists of D-flipflops, multiplexers and adder designed for 16 dimensional vector. During image encoding mode s1 is set as 0. The values of $(x_j\text{-}w_{ij})^2$ were computed by SDU and then transmitted to Binary Adder Tree. Sum up all of the partial SED_s to get exact SED is done. During last stage the separation signal "S_{SEP}" is "0" until all partial vectors processed. Exact value of SED is obtained when "S_{SEP}"turns to "1"and it is fed to minimum distance search circuit where searching for winner neuron is done. During codebook learning "s1" is set to "1" when winner neuron searching phase is completed. In read port of codebook memory the

 DOI : 10.35291/2454-9150.2020.0159

beginning address of winner neuron is loaded and then sixteen dimensional partial weight vectors of winner neuron read out in sequence.

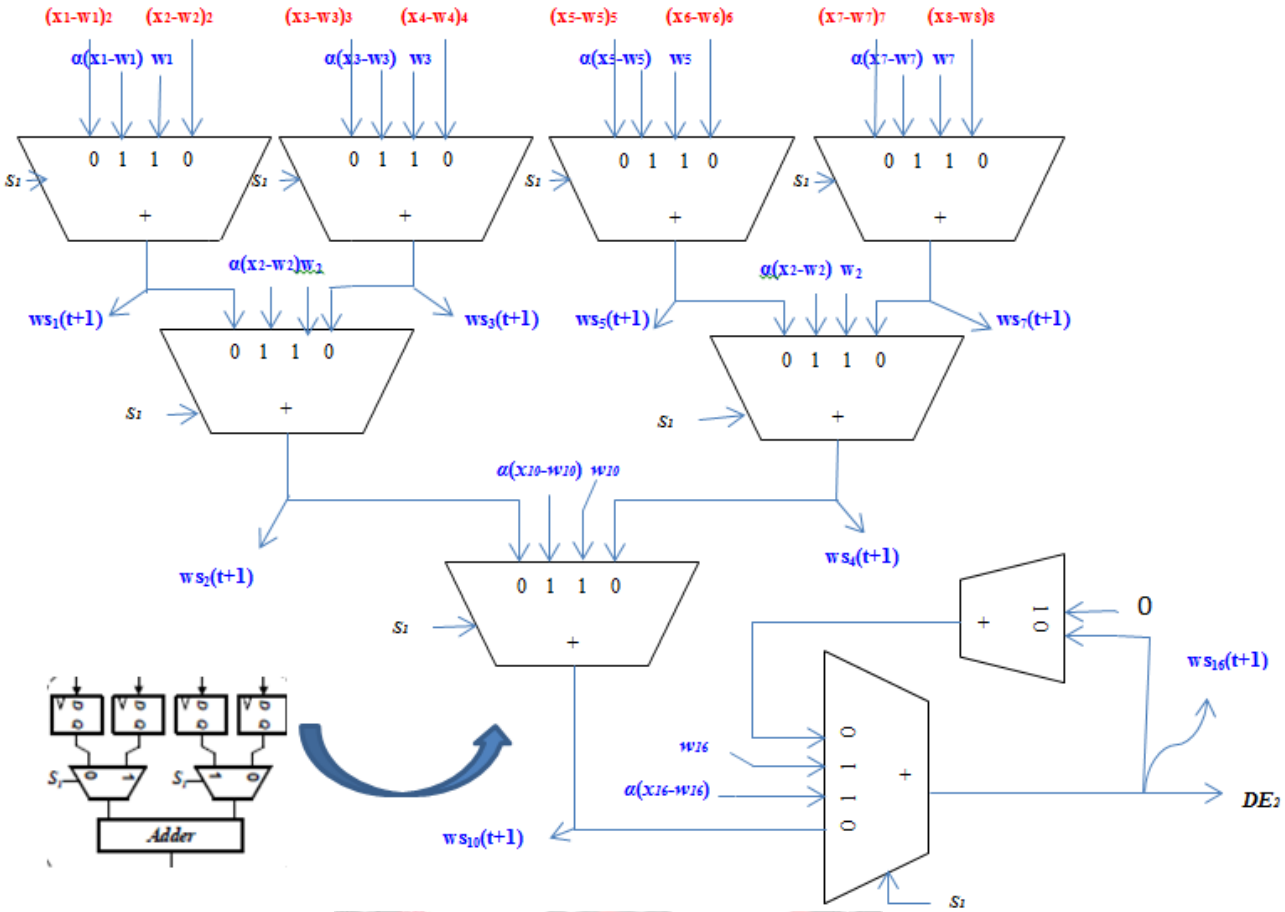

Fig.4: Complete binary adder tree circuit

Minimum Distance Search Circuit is implemented to find winner neuron the distances between in out vector and all of the weight vectors computed and the compared with each other. Winner-takes-all circuit (WTA) executes the operation of minimum distance search.This block consists of shift register, comparator, AND gates and D flip-flop. The exact SED from adder circuit is fed as in put to WTA circuit, the signal S_{SEP} act as separate signal for other SED_S,during winner neuron searching phase minimum SED and its corresponding address stored in R2 and R3 temporally. Newly arrived SED 'DE^2' is loaded in R1and compared with minimum intermediate SED when "S_{SEP}" is "1". If '$DE^{2'}$ is smaller values in R2 and R3 will be update. After the searching of weight vector, in codebook memory start address current weight vectors is stored will be output as an index.

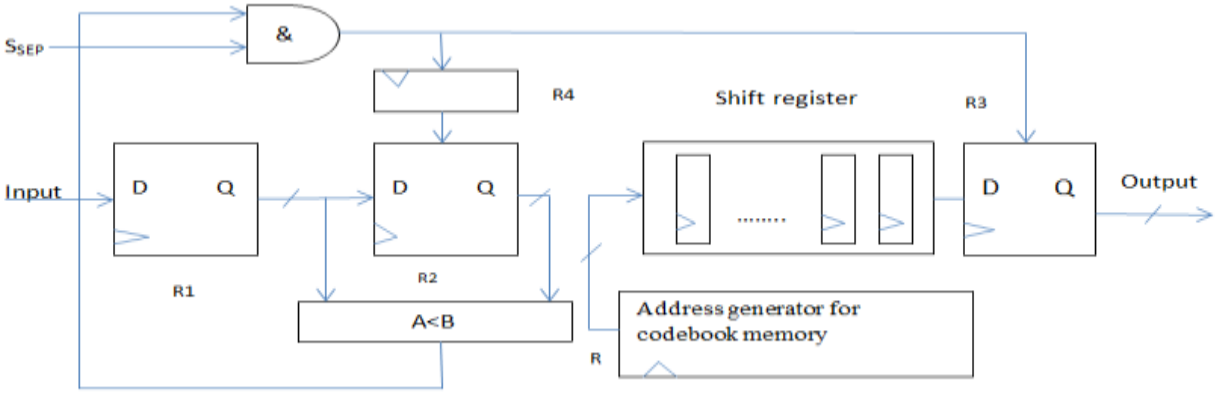

Fig.5: Block diagram of the winner-takes-all circuit

 DOI : 10.35291/2454-9150.2020.0159

V. RESULTS AND DISCUSSION

ASIC parameters such as power, area and delay are calculated for each block using the CADENCE EDA TOOL in 90nm technology. The circuit parameters are shown in the below table 1.1.

Table 1. ASIC parameters for blocks of vector quantizer

BLOCKS	AREA(nm^2)			POWER(nW)			DELAY (ps)
	CELLS	CELL AREA	TOTAL AREA	LEAKAGE POWER	DYNAMIC POWER	TOTAL POWER	
Squared Distance Unit	8	823	823	114.466	114.069	228.535	12
Reconfigu -Rable Binary Adder Tree	16	2134	2134	129.421	129.594	259.015	19
Minimum Distance Search Circuit	16	2325	2325	137.621	137.813	275.434	27

Image compression is implemented using Linde-Buzo-Gray algorithm to the digital image of size 512*512 UNIT8 it results the compressed image of size 256*16 double in MATAB.

Table 2.Original And Compressed Images of Clustering Method

Input Images Compressed Images

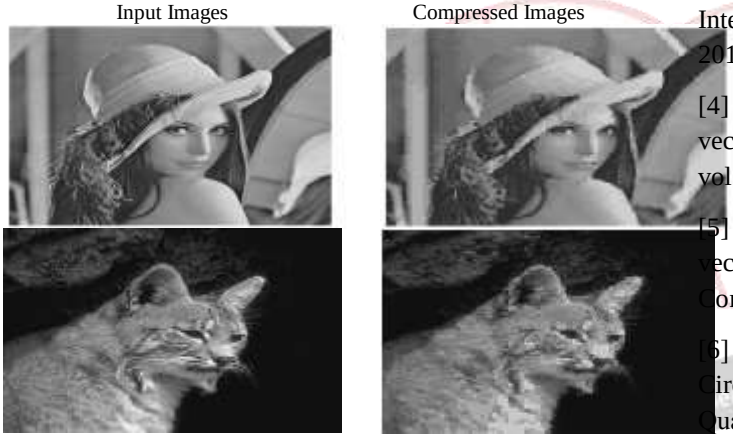

Table 3.Original and Compressed images of Modulus Method

Input Images Compressed Images

The PSNR values of Clustering and Modulus method is obtained as 38.0618 and 28.5194.The nominal value is about 30 db to 50 db.

IV. CONCLUSION

In this paper, image compression is implemented using VQ technique. Blocks like Squared Distance Unit, Reconfigurable Binary Adder Tree, Minimum Distance Search Circuit unit needed for processing 512*512 image is designed using verilog HDL. From this optimized value of parameters such as area, power and delay has been calculated using 90nm gpdk technology in CADENCE-EDA tool.

REFERENCES

[1] Zunkai Huang, Xiangyu Zhang, Lei chen and Fengwei An,"A Hardware-Efficient Vector Quantizer Based on Self-Organising Map for High Speed Image Compression" Applied Sceince,2017.

[2] J. Han, H. Chen, J. Liang, P. Zhu, Z. Yang and F. Lombardi, "A Stochastic Computational Approach for Accurate and Efficient Reliability Evaluation," IEEE Transactions on Computers, vol. 63, no. 6, pp. 1336 - 1350, 2014.

[3] P. Li, D. J. Lilja, W. Qian, K. Bazargan, and M. D. Riedel, "Computation on stochastic bit streams digital image processing case studies," IEEE Trans. on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 3, pp. 449-462, 2014.

[4] Y. Linde, A. Buzo and R. M. Gray, "An algorithm for vector quantizer design."IEEE Trans. on Communications, vol. 28, no.1, pp.84-95, 1980.

[5] N. M. Nasrabadi and R. A. King, "Image coding using vector quantization: A review." IEEE Trans. on Communications, vol. 36, no.8, pp 957-971, 1988.

[6] R. Wang, J. Han, B. Cockburn and D. Elliott, "Stochastic Circuit Design and Performance Evaluation of Vector Quantization," in Proc. IEEE ASAP 2015, IEEE 26th International Conference on Application-specific Systems, Architectures and Processors, Toronto, Canada, July 27 - 29, 2015.

[7] R.M. Gray, Vector quantization, IEEE Signal Process. Mag. 1 (2) (1984) 4–29.

[8] D. Ailing, C. Guo, An adaptive vector quantization approach for image segmentation based on SOM network, Neurocomputing 149 (2015) 48–58.

[9] G.E. Tsekouras, A fuzzy vector quantization approach to image compression, Appl. Math. Comput. 167 (1) (2005) 539–5605.

 DOI : 10.35291/2454-9150.2020.0159