PERFORMANCE EVOLUTION OF THE SUB 20 nm FinFET BASED INVERTER CIRCUIT

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Abstract In this paper, an inverter circuit is analysed to understand the circuit behaviour of a fully depleted SOI FinFET device, which has been a promising substitute for the conventional bulk CMOS based device in the nanoscale regime. The performance of the sub 20 nm based FinFET inverter circuit by considering the delay and power dissipation of the basic inverter circuit is studied. FinFET devices are extensively used by most of all designers due to its better controllability of the channel by gate terminal, reduced short channel effects and high ION/IOFF. This paper portrays the FinFET device modelling and the device is used to study the circuit performance. The delay and power consumption are evaluated in comparison with the sub 14 nm and 22 nm standard technology nodes.

Keywords- FD SOI FinFET, H-Spice, Inverter, delay performance , power consumption.

I. INTRODUCTION

Since post 90's it has become more apparent to switch to the new novel technique like Multi-gate MOSFETs and Silicon on insulator substrates providing more credibility in the fabrication of semiconductor devices. The speed and power advancements recuperate by employing these novel device techniques. By adaptation of SOI substrates in the fabrication of semiconductor devices like microprocessors, memories have inclined more thrust to research in SOI. The success in SOI technology gave more credibility in the manufacturing of semiconductor devices. The classical CMOS device structures run to the scaling limits and end of the road map. Henceforth alternative device structures are being investigated such as multiple-gate field-effect transistors (Multi-gate FETs) [1-4], Carbon nano-tube field-effect transistors (CNT FETs) and tunnel field-effect transistors (TFETs)[5-9].

SOI devices tender the advancement of improved drive current, lowered parasitic capacitances and are highly immune to short channel effects. As the dimensions of the semiconductor devices are scaled the performance of the devices are more affected by the short channel effects. These device parameters vary due to the geometrical dependent parameters like silicon thickness, oxide material and thickness of it, doping concentrations[10-15].

Considerable research has been carried due to the advantage of the SOI-based FinFET device. The circuit-level implementation is studied and compatible through Look Up Table based models. Different research has been carried outbased on Predictive technology model and BSIM model for sub 20 nm technology nodes [16-18]. Verilog A implementation is carried out by using a Look-up-table (LUT) of FinFET devices which is compatible for SPICE simulations for analysing the circuit performance of the FinFET based models [19-21].

The rest of this paper is organised as follows, Section II introduces the surface potential based analytical modelling of FinFET devices at multiple bias voltages. Section III demonstrates the LUT based H-spice circuit design flow. The power density reports as well as synthesis results of the inverter are narrated Section IV and concludes the paper in Section V.

II. ANALYTICAL MODELING

The 3-dimensional view of Tri-gate FinFET is shown in Figure 1.a and 2-dimensional cross-sectional view is shown in Figure 1.b where L_{Fin}, W_{Fin}, H_{Fin}, t_{ox} and t_{box} are the Length, Width and Height of the channel, oxide thickness and buried oxide thickness respectively. It is assumed that movable charge carriers are neglected and source, channel & drain region jumps are abrupt in FinFETs when operating at sub-threshold region. Table 1. shows all the device parameters of Tri-gate FinFETs [22].

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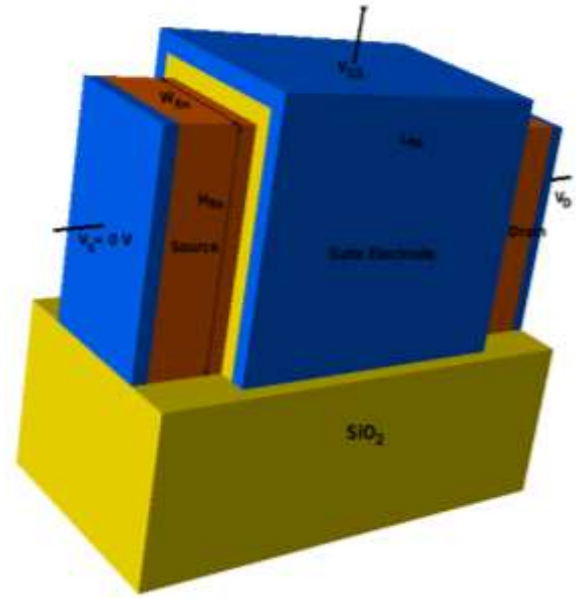

Figure 1.a 3D view of Tri-gate FinFET

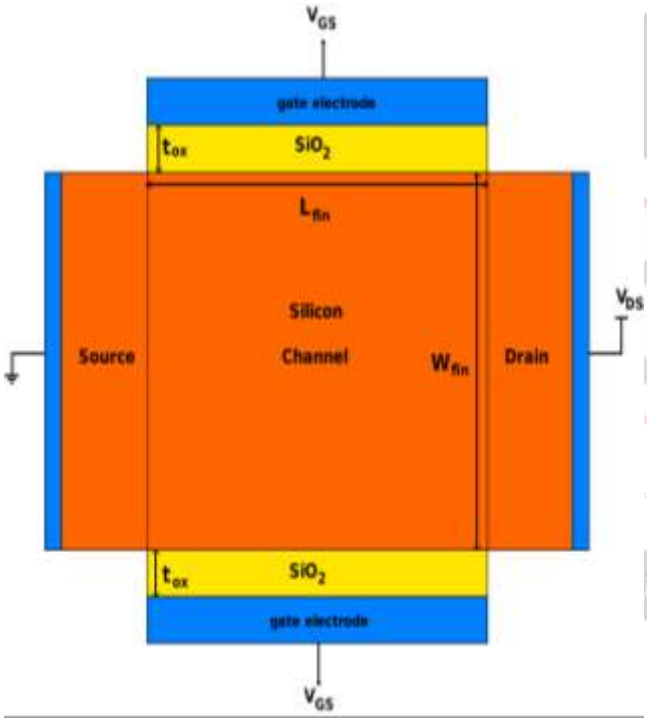

Figure 1.b. 2 Dimensional view of FinFET

Table 1. Geometric Parameters for FinFET.

Sl.No	Parameter	Symbol	Value
1	Length of Fin	L_{Fin}	20 nm
2	Width of Fin	W_{Fin}	10 nm
3	Height of Fin	H_{Fin}	10 nm
4	Oxide Thickness	t_{ox}	1 nm
5	Buried Oxide Thickness	t_{box}	20 nm
6	Gate Work function	φ_G	4.7 eV
7	Source/Drain Work function	φ_{SD}	4.1 eV
8	Source/Drain Doping	$N_{S/D}$	10^{19} cm^3
9	Channel Doping	N_C	5×10^{17} cm^3

Based on the previous work, the solution to the two dimensional Poisson's equation is analytically modelled by considering mobile charge carriers is discussed in this section [16]. Fig.1.b. shows the 2D cross-sectional view of the FinFET in *x-y* plane and is given by,

$$\frac{d^2\varphi}{dx^2}+\frac{d^2\varphi}{dy^2}=\frac{q}{\varepsilon_{Si}}n_i e^{\frac{\varphi-V}{V_t}} \quad (1)$$

Where the electrostatic potential across the channel region can be defined as, $\psi(x,y)$, thermal voltage V_t = *0.0259 V*, the intrinsic carrier density is n_i and *V* be the quasi-Fermi potential. By employing the superposition principle, electrostatic potential can be given as

$$\varphi(x,y)=\varphi_x+u_L(x,y)+u_R(x,y) \quad (2)$$

Where the solution to the 1D Poisson's equation can be given as ψ_x and $u_L(x, y) + u_R(x,y)$ is the solution to the 2D Laplace equation.

Based on the analytical surface potential model, refereeing Pao and Sah's double integral Equation to drain current is calculated by,

$$I_{DS}=\mu_{eff}\frac{W}{L}\int_0^{V_{DS}}[-Q_i(V)]dV \quad (3)$$

Where $Q_i(V)$ is inversion charge, a function of *V*.

The Transconductance model is the electrical property of the device and shows the sensitivity of the device i.e. how fast the current will increase for a short duration of input voltage. Transconductance is denoted by g_m and is calculated by

$$g_m=(\partial I_{ds}/\partial V_{gs})\big|_{Vds} \quad (4)$$

Based on the analytical modelling which is carried in the previous research work is briefed in this section. The characteristics for Tri gate FinFET is validated with a 2-dimensional numerical device simulation tool and raw data are extracted from a TCAD simulation tool.

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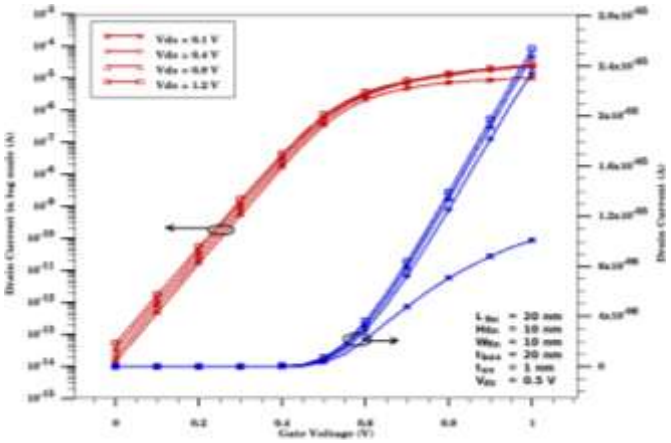

Figure 2.Transfer characteristics in both linear and logarithmic scale for different drain bias (V_{DS}).

Figure 4 shows the *V-I* characteristics in linear scale and logarithmic scale for distinct drain biases respectively, linear part of *V-I* characteristics shows the higher value of drain current for higher input drain bias, which also shows the current variation along with the input biases. The logarithmic scale of *V-I* characteristics shows the off current (I_{OFF}) as well as on current (I_{ON}) of the device. The performance of the device is gauged by the higher I_{ON}/I_{OFF} ratio. Our model shows an OFF current of 10^{-14} *A* and ON current of 10^{-5} *A* with I_{ON}/I_{OFF} ratio of around 10^{9} for drain bias of *0.4 V*.

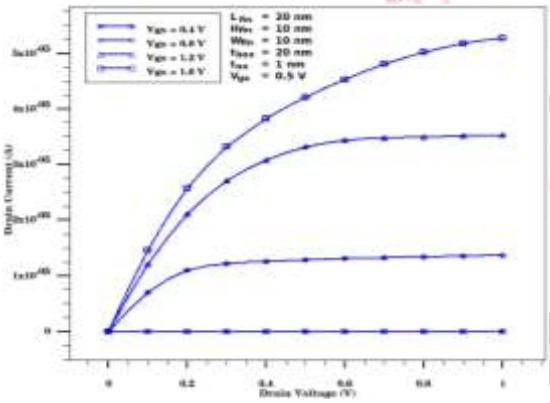

Figure 3.Output characteristics for different input biases.

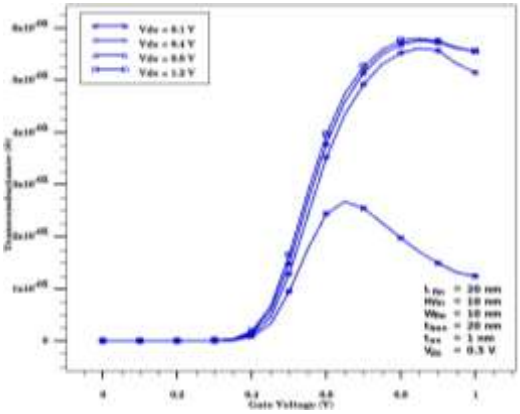

Figure 4.Transconductance plot for FinFET.

Figure 3 shows the plot for output characteristics for Tri-gate FinFET for varied input gate bias. It shows no current for the input gate (0.4 V) to source voltage less than the threshold voltage (0.42 V). It shows constant drain current for input voltage less than 1.2 V, after reaching the saturation point for drain saturation voltage V_{DSat} . For the input voltage above 1.2 V the channel undergoes channel length modulation and with effect to this output current starts increasing linearly with respect to drain bias.

Figure 4 shows the AC parameters such as Transconductance and Output Conductance of the Tri-gate FinFET. Figure 4 represents the plot of transconductance for Tri gate FinFET. The results analysis is explained in the previous research work [22].

III. LUT BASED HSPICE DESIGN FLOW

In this sub section, an inverter circuit is implemented using our proposed FinFET model. Since the circuit level performance of the modelled device is verified by creating 2D lookup tables of I_{DS} and g_m as a function of V_{GS} and V_{DS}. all the lookup table data is obtained by a 2D numerical simulator, Silvaco TCAD tool. The obtained 2D lookup tables are further executed in Synopsis H-spice tool to get the circuit behaviour of the inverter circuit, Verilog-A model is used for designing a FinFET based inverter circuit as a part of designing semiconductor memories applications. Fig. 5 represents the device and circuit simulation framework over which circuit behaviour is studied.

The circuit simulations are carried out using H-Spice simulation tool by Synopsys and an optimized circuit simulator. The electrical characteristics of the inverter circuit are simulated in the transient domain. H spice is the finest adaptation for accurate and fast circuit simulation and expedites the circuit-level analysis with the concern of the performance.

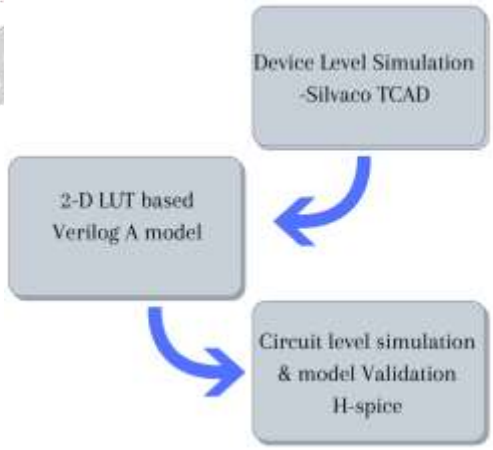

Figure 5. Device to circuit-level simulation flow.

Numerical simulation of the inverter circuit is dependent on the finite element methods. Silvaco TCAD simulations are useful for design investigation and technology evaluation of FinFET based circuits. The model employs the physical expressions to capture the effect of device parameters such as L, H_{fin} and W_{fin} on various electrical characteristics of multi-gate MOSFETs. The FinFET device which is carried in this work with 20 nm technology.

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The design consideration is one of the prominent steps in evolving with a spice model and simulating it. The design parameters are extracted from the numerical 2D TCAD simulator with the above mentioned geometrical parameters in table 1. Node technology is interpreted based on the length of the gate, as the device geometry and the supply voltage is scaled down as per the rule of technology scaling to meet the design requirements.

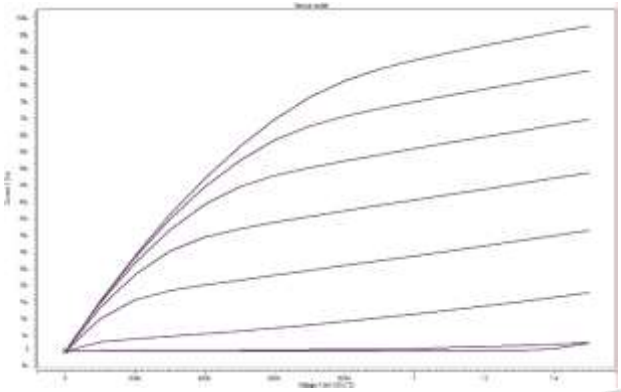

Figure 6(a) Output characteristics for n channel FinFET

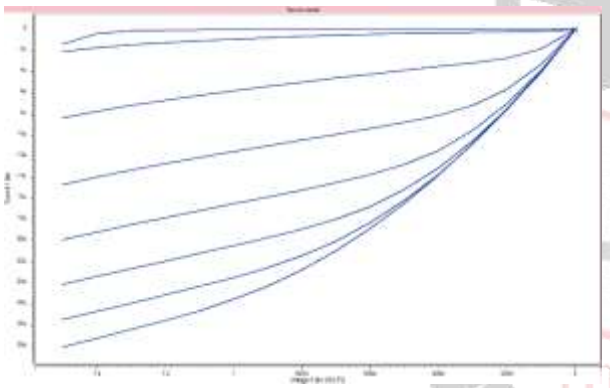

Figure 6 (b) Output characteristics of a p channel FinFET

I_D-V_{ds} characteristics for n-channel and p-channel *FinFET* are shown in figure 6. It shows the behaviour of drain current for various drain bias with reference to different input voltages. Based on the characteristics a basic inverter circuit has been realized in this subsection and is more capable of evaluating device performance.

IV. POWER AND DELAY ANALYSIS

To design any of the digital circuits one must need a very good understanding of basic CMOS inverters, with the understanding of operation and properties of any inverter circuit can help to extend the digital logic design and semiconductor memories. A basic inverter circuit is a key parameter to analyze any VLSI circuit, it is the fundamental circuit which is more suited to analyze the circuit performance of the device for the particular technology node.

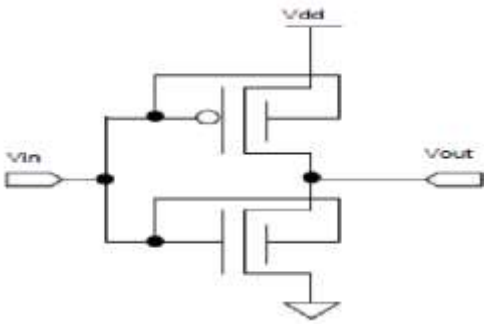

Figure 6. A TFET based inverter circuit

Figure 6 depicts a basic inverter circuit as shown; the structure consists of a simple combination of *pMOS FinFET* at the top, the source is associated with V_{DD} and a *nMOS FinFET* at the bottom with the source connected to the ground. Gate terminal of both the transistors is put together to the Vin and drain of both the transistors are connected to the V_{out} terminal.

VTC Curve

The prominence of the digital inverter is measured by the voltage transfer characteristics (also referred as voltage transfer curve) shown as an inverted step function, this will indicate the precise switching between on and off states. VTC indicates a lower input voltage gives rise to higher output. The slope of the transition region is a measure of quality; steep slopes yield precise switching.

Figure 7.a shows the voltage transfer curve for the FinFET based inverter or DC characteristics of an inverter. The voltage transfer characteristics are divided into five regions. The optimum operation is achieved when $V_{in} = V_{DD}/2$ we get the output $V_{out} = V_{DD}/2$. The threshold voltage of the proposed model is V_{TH} = 0.4504 V with the operating voltage V_{DD} = 1.5 V. This is achieved by adjusting width and length of both nMOS and pMOS as other parameters like mobility, oxide capacitance which vary between different technologies.

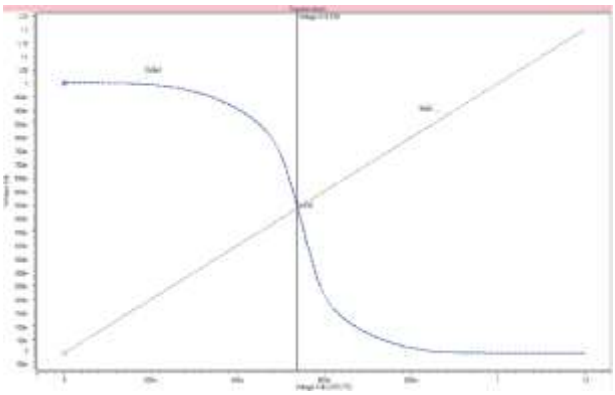

Figure 7. (a) VTC curve for Inverter

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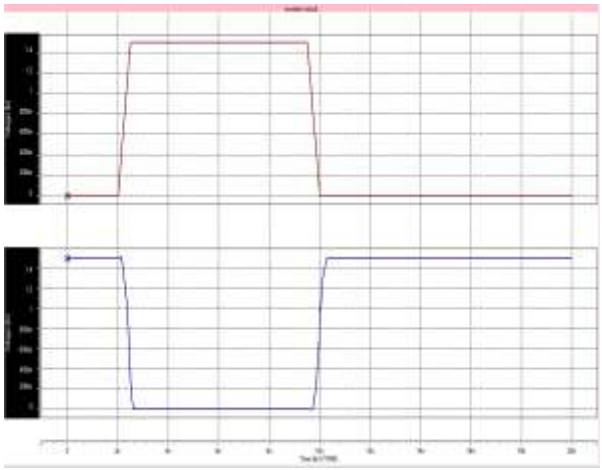

Figure 7 (b) Input and output voltages for an Inverter

The rising time and falling time of the circuit describes the delay of the FinFET based inverter, that can be measured in terms of

$$\text{Delay} = (\text{Rise time (tr)} + \text{Fall time(tf)}) / 2 \quad (5)$$

The important parameter for measuring the stability of any digital circuit is the noise margin of an inverter. Noise margin is identified as the highest allowable which is accepted by a device when utilized in any system. For an inverter, the voltages V_{OH}, V_{OL}, where V_{OH} is the minimum output high voltage and V_{OL} is the maximum output low voltage, similarly, V_{IH}, V_{IL}, where V_{IH} is the minimum input high voltage and V_{IL} is the maximum input low voltage, thus high and low state noise margins can be mathematically defined as

$$NM_H = V_{OH} - V_{IH} \quad (6)$$

$$NM_L = V_{IL} - V_{OL} \quad (7)$$

To assure the competent operation of an inverter, the noise margins must be sufficiently positive and are directly associated with the reliability and robust operation of the logic circuits. Based on the VTC curve shown in fig 7.a delay of the circuit can be modelled and furthermore it can be implemented for logic circuits and semiconductor memories.

Figure 7.b shows the input and output characteristics of the proposed 20 nm FinFET based Inverter circuit. As for low input, the value reads a high output value. The delay of the circuit is characterized by the rise time and fall time of the pulse.

Table 2. comparison analysis of delay and power dissipation

PARAMETER	14 nm FinFET Inverter	22 nm FinFET Inverter	20 nm FinFET Inverter
Delay	74.0142 ps	45.4625 ps	42.0654 ps
Power Dissipation	393.9912 fW	414.8270 fW	452.0343 fW

Power consumption and dissipation is also an important performance parameter in the implementation of digital circuits. Power consumption is categorized into static & dynamic power consumption. The rate of switching of the logic levels from high to low and low to high reads the switching power. The off state of the circuits leads to the leakage power and is summed up by the power dissipation of all the cells that are not being powered in the circuit.

Delay and power consumption of the FinFET based design of the proposed model is compared with the standard 14 nm and 22 nm FinFET inverter and shows better agreement in comparison with the standard model.

V. CONCLUSION

Fully depleted SOI FinFETs are a promising alternative for bulk CMOS for converging the defiance being posed by the scaling of conventional MOSFETs. The proposed model shows the performance evaluation of the FinFET based inverter circuit resulting in better delay and power optimization. The model is validated with standard 14 nm and 22 nm FinFET based Inverter circuits. The proposed model reads a threshold voltage of 0.4505 V for a supply of V_{DD} = 1.5 V and reads an inverter delay of 42.0654 ps with a power dissipation of 452.0343 fW.

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