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High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations with Efficient and power optimized pattern generator for High-Speed applications

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Abstract: **This paper introduces the development of experimental models using the low-resolution version of the BIT-SWAPPING LFSR, which reflects the desired conversion rate faster than traditional pseudo-dimensional models by reducing the conversion rate to the desired level. The proposed design produces efficient and powerful test models and minimizes overall change performance that can reduce overall overall time delay. This concept proposes an alternative approach to constructing the transition matrix used in state transformation. Introduced a complete search algorithm to search for the right matrix for the right transition. Small complex structures are often found, which supports the restoration of this improved state. The continuity of the program is enhanced by scan chain re-order technique to further improves the delay parameters. Scan chain reordering means, reordering the inputs in such how that the amount of transitions in input and output is extremely less, with this switching activity, it leads to optimize the power of overall circuit compare to previous method. This reduces the number of changes (i.e. switching's) in the scan-chain input during the scan shift operation compared to those patterns produced by the standard LFSR.**

IndexTerms **- Bit-swapping Lfsr, Scan chain reordering, state space transformation, circuit under test.**

I. INTRODUCTION

There are different components that influence the estimation of chip like bundling, application, testing and so forth In VLSI, predictable with thumb rule half of the whole coordinated circuits cost is on account of testing. since the VLSI plans increment in incorporation thickness, related modules become blocked off and testing of the chip gets troublesome. at the point when outer ATE is utilized for testing, the test business is confronting numerous issues like expansion in test time. To influence this, Test age gear can lessen the need for test access for worked in individual test (BIST). An overall kind of BIST structure is given in Figure.1. Test design age and yield reaction analyser are simply the 2 significant capacities that help in self testing of circuit under test (CUT) by BIST. Test design generator produces grouping of examples to be applied to hack for testing. Yield reaction analyser (signature analyser) contrasts the encoded yield of CUT and anticipated yield and shows whether the circuit is broken or deficiency free.

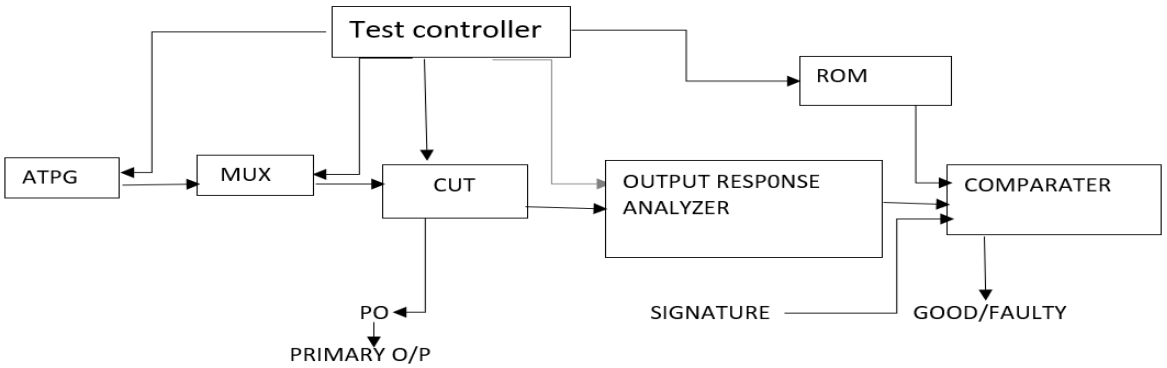

FIGURE 1: BUILT IN SELF TEST

Input isolation circuitry prevents the critical time system inputs to go into the CUT, while the system is in check mode. Test controller is subjected to be accountable for beginning of the layout earlier than check inputs have been carried out and additionally as earlier than output responses are given for compaction. The check era technique is extensively utilized

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in Built in self-check-primarily based totally bit swapping linear comments register. The form of check styles that allows you to be taken into consideration in our take a look at are going to be pseudo exhaustive the usage of LFSR. First identity of feature polynomial, that desires decrease range of seed to deliver all viable styles, has been studied in detail in [1]. Flip-Flops are the basic unit for constructing LFSR. Initially flip-flop ought to be loaded with the seed price and while the LFSR is clocked, it's going to generate random check sample which can be used as check vectors in BIST. With right faucet sequence, LFSR can generate random check sample which achieves excessive fault insurance in the course of a exceedingly quick run of check vectors. Power dissipated in the course of checking out is extra in contrast to electricity ate up through the circuit in the course of ordinary running mode.

Hence, it's miles ideal to optimize the power ate up for checking out any VLSI circuit. Reversible common sense is one most of the strategies to reduce the power dissipated through the circuit. it is one to as a minimum one mapping among enter and output (Viz: it is continually viable to get better the enter from output and vice versa) and therefore there will be no records loss. Irreversible circuits result in extra cooling way to records loss. Thus, through enforcing LFSR the usage of reversible common sense power dissipation are frequently decreased and consequently the identical LFSR are frequently need to design power efficient BIST architecture.

II. REVIEW OF PREVIOUS WORK

Linear feedback shift registers LFSRs) are widely used in BCH and CRC encoders to calculate the remaining polynomial. The standard BCH (n, k) code encoding system is shown in Fig. 1. Although such serial LFSR configurations can work at very high frequencies, there is a problem with serial-in and serialout limits. Where the performance of this serial architecture cannot detect system data rate, the same processing should be considered to meet the general speed communication requirements and obtain a higher throughput rate of more than gigabits per second as optical transmission. Certain types of compact LFSR formats have already been introduced in the related BCH and CRC encoders. In [10], the same CRC implementation has been designed with statistical drawings. Tree calculations and subexpressions are accepted to enhance the logical parts of the mind. Parhi [11] and Zhang and Parhi [12] have proposed an advanced BCH high-speed codec designed to eliminate the fanout bottle. This method of building LFSR works well for speeding up computer calculations, but its hardware costs are high. A state-of-the-art transformation model is developed at [13] and [14] to reduce the general complexity of the corresponding CRC circuits. By adopting a specific matrix conversion, a full-speed feature can be obtained at an additional circuit cost without a response. Ainala and Parhi [15] and Jung et al. [16] suggested another type of compatible LFSR based on IIR topology filtering and its advantage is that the piping process can be used to achieve some improvement in the hardware efficiency of LFSR encoders.

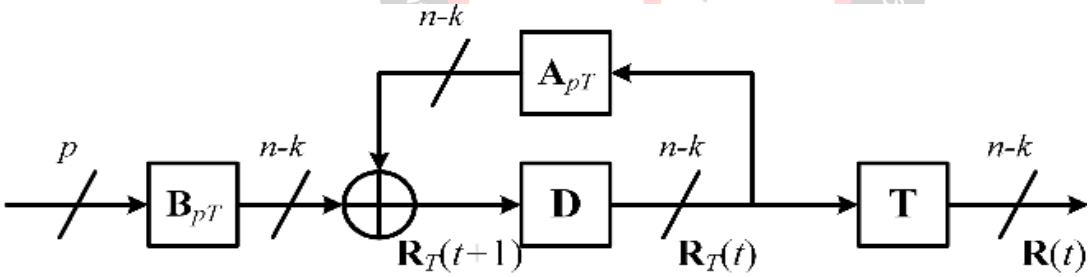

Fig. 2. Block diagram of the parallel LFSR architecture applying state-space transformation.

III. PROPOSED WORK

3.1 PROPOSED BUILT IN SELF TEST PATTERN GENERATOR

The block diagram for Built in Self-Test Pattern Generator proposed architecture is shown in fig 3.1. Two test pattern generators are generated by Built in self-test test pattern generator,1) Low Transition BIST and 2) Adder based Weighted random BIST. The Multiplexer is used to select the input source between LT-BIST and A3WRBIST using selected line. In the first section the test patterns, which are generated by LT-BIST are selected by multiplexer and scanned too, for easy to detect faults. In the second section, the test patterns are which are generated by A3WRBIST which are selected by multiplexer and scanned too, to detect the remaining faults which are left by LT-BIST. Here, the LT-BIST will be implemented by one T-FF and one AND gate with standard LFSR which give low hardware to design the circuit.

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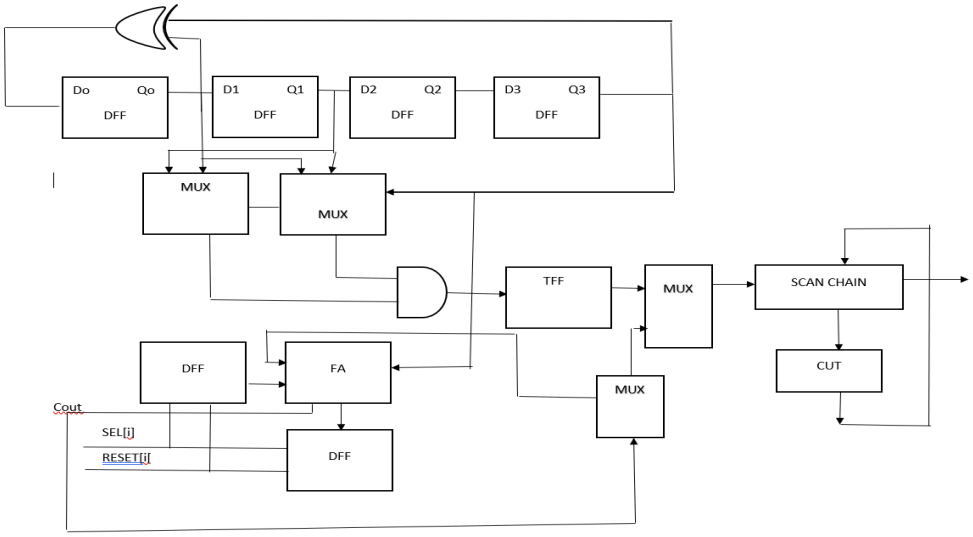

FIG 3.1: PROPOSED BIST- BS LFSR

The complete Hardware to implement to generate the pseudo random pattern is depends on giving the input logics of A3WRBIST.The A3WRBIST is consists of one -FA and two D-FFs. So, the by using above two circuits for test pattern generator which will reduce the total area required to design the low power bit swapping LFSR circuit which may leads to reduce the total power consumption compared with Existed High speed parallel LFSR. The proposed method is known as bit-swapping LFSR (BS-LFSR), consists of an LFSR with data flipflops and a 2*1 multiplexer. It is used to reduce number of switching activities to more than fifty percent by producing scan based BIST when compared to those patterns produced by a conventional LFSR. These techniques have a substantial effect on average time reponse and peak-power reductions with negligible effect on fault coverage or test application time.

3.2 BIT SWAPPING LFSR

The diagram of Bit-Swapping Linear Feedback register architecture in shown in fig 3.2. The functioning of Bit-Swapping Linear Feedback register is counting on basic bit swapping method is given to the output sequence of a standard LFSR and implemented employing a traditional LFSR and a 2:1 MUX. BS-LFSR is usually implemented to attenuate the typical and instant Weighted Transition Activity during test function by minimizing the amount of switching at the scan input of the CUT. The pseudo random patterns are generated by the Bit Swapping LFSR which is employed to acknowledge easy-to-detect errors. The working rule of figure 4.2 is depends on the subsequent polynomial

$$Xn \text{ ^1+1}$$

Value of "n" during this work is "4" (Depends on the CUTs inputs) for instance, the worth of "n" is chosen as 4 and therefore the LFSR is given with 1010, then Linear Feedback register started the activity of generation of pseudorandom test patterns. C1 and C2 are swapping bits and Cn bit is taken as feedback from X-OR circuit to C1 bit. If the worth of Cn bit are going to be "0" then two bits are going to be swapped. If value of Cn gets "1" then two bits are remains because it is. Therefore, Cn bit is employed as selection line for 2:1 multiplexer.

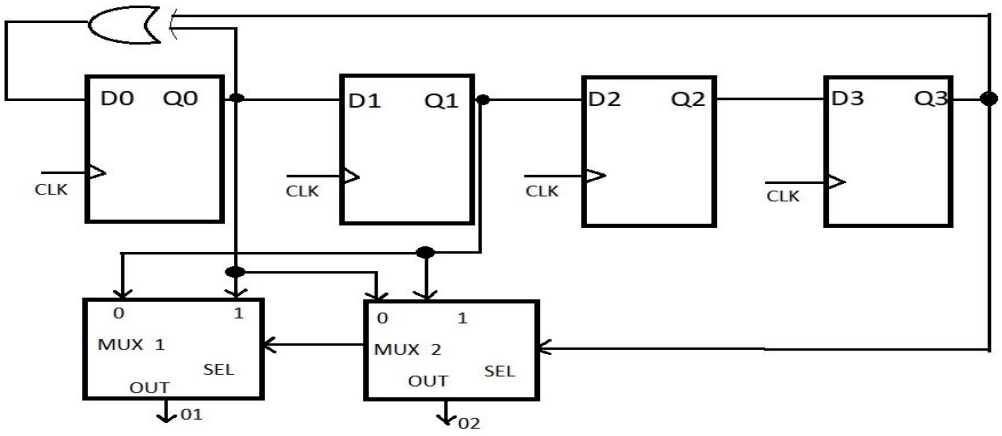

FIG 3: BIT-SWAPPING LFSR

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The 2:1 multiplexer is usually wont to minimize number of switching happens at the input of the scan chain, in order that the facility consumption is minimized during the test time. The length of the LFSR is 4 and consequently 16 combinations are probable. BS-LFSR additionally generates 16 combinations those are same as LFSR generated patterns however only variation is that the situation of the combinations is modified. the number of switching's present within the test patterns produced by both LFSR and BS-LFSR are in contrast and computed.

3.3 SCAN CHAIN

There are so many methods for reordering mechanism of scan cells which are used to arrange order of test vectors leads to reduction in switching activity, Based on the routing constraints scan chain reordering mechanism is used to design for low power scan chains by arranging their order of scan test vectors, and order of scan chains and order if both test vectors and scan flipflops. The forming clusters, reorder scan cell within a cluster and cluster reordering are the basic steps of this method. Another method for recording mechanism is based on switching frequency-based method. This method is used to reduce a huge amount of power dissipation during test time by changing the internal scan test ordering test inputs. Few methods are used to develop the transition weights and few other methods are used to calculate the transition effects at scan cells at circuit under test during switching activity. The proposed LT-BS-BIST is successful get minimizing the transitions present at input of the scan and test vectors other than this any other mechanism is not suitable. The below algorithm is developed for minimizing the transitions in the scan chain by loading the test vectors.

Scan chain vectors/responses	Flipflop 1	Flipflop 2	Flipflop 3	Flipflop 4
V1	1	0	0	1
R1	0	1	0	0
V2	0	1	0	1
R2	0	0	1	0
V3	1	1	1	1
R3	1	0	1	1
V4	1	0	1	0
R4	1	0	0	1

Fig.4: Calculation of Transitions for the deterministic test vector of s-27

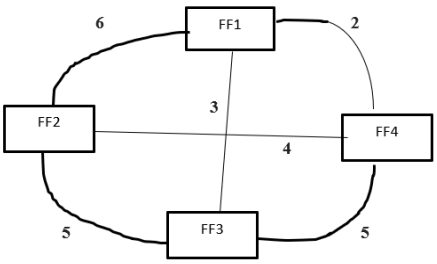

Fig 5 : Graphical representation of transitions of s-27

To determining the order of scan cells in scan chain for s27 standard bench mark circuit. Consider the four test vectors V1, V2, V3 and V4 and the response of Circuit under Test for the Test Vectors are R1, R2, R3 and R4. The length of the scan chain is equal to number of test vectors. Therefore, the number of scan cells in the scan chain re four givens in fig 5.8. For Every scan cell are made with one Flipflop so that for four scan cells requires four Flipflops called FF1, FF2, FF3, FF4. **A low transition built-in self-test (LT-BIST) or built-in test (BIT**) block diagram is shown in fig.6 is mostly implemented to minimize the transition activity during BIST functioning, by minimizing the switching take place at input of the scan chain during scan shift functioning. The LTBIST is 86 contains of an n-stage BS-LFSR, a L-input AND gate, and a Toggle-FLIP FLOP. Therefore, it can be implemented with a less hardware. Every "L/K" inputs of the AND gate is given the LFSR. If large value of K is used, a greater number of sets of adjacent state inputs will be assigned same values in most test patterns, leads to decrease the fault coverage or the

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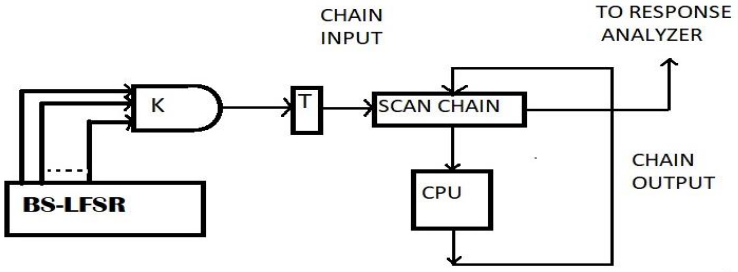
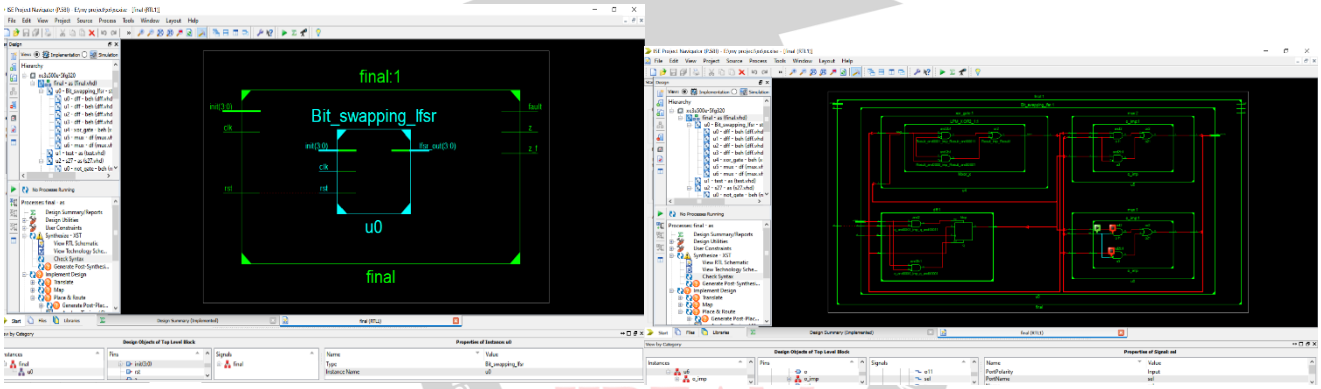


Fig 6: Low Transition BIST

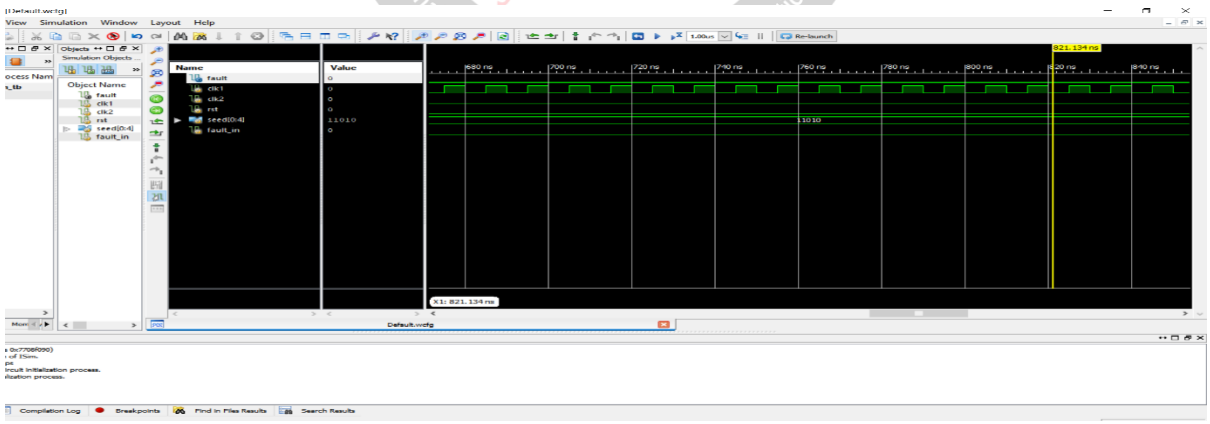
improves in test sequence length. Although LTBIST is successful in minimizing the number of switching which happens at the input of the scan chain which again leads to minimizing in heat dissipation during overall scan testing. As adjacent scan flip-flops are assigned same values in max test patterns, the consecutive test patterns produced by LTBIST has contains less correlation. This less correlation leads to minimize the fault detection capability of LTBIST. Therefore, LTBIST is mostly implemented to recognize easy-to- detect errors. The faults which are descend by Low Transition BIST, are known as Random Pattern Resistant Faults (RPRFs).

IV. SIMULATED OUTPUT RESULTS

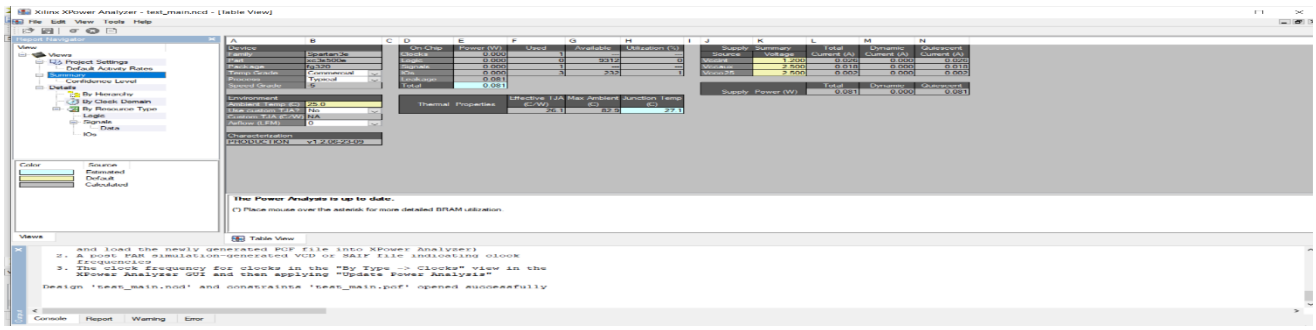
4.1 RTL SCHEMATIC VIEW



4.2. SIMULATED OUTOUT WAVEFORMS



4.3. POWER ANALYSIS



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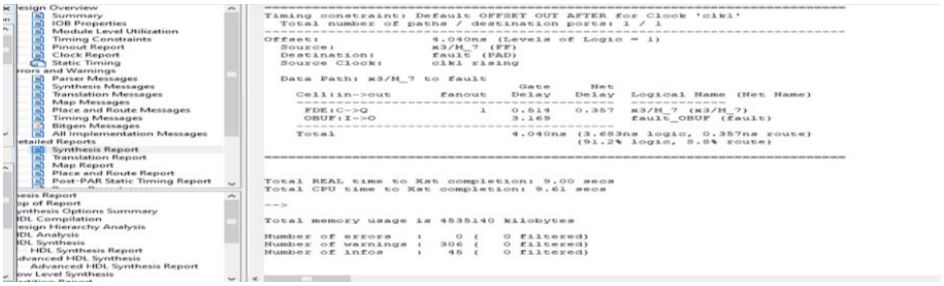
4.4. TIME ANALYSIS



V. CONCLUSION

A low-transition proposed TPG is employed to get test patterns by using scan BISTs so as to scale back the amount of transitions activities while drive test vectors into the scan chain. Moreover, a completely unique algorithm for scan-chain ordering has been presented. When the BS-LFSR is employed along side the proposed algorithm, the typical and peak powers are substantially reduced. The effect of the proposed design within the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previous methods show that the proposed design are able to do better results than previous methods.

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