International Journal for Research in Engineering Application & Management (IJREAM)
ISSN : 2454-9150 Vol-06, Issue-12, MAR 2021

A Novel Pseudo PMOS Integrated Low Power Inductor less LNA used for Wireless Receiver

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Abstract **A performance study of a novel Pseudo-PMOS integrated LNA used for wireless receiver with zero static power dissipation is presented in this paper. The simulation of power and performance measurement, as well as comparisons with existing systems used in wireless receivers, is the key focus. The commonly used devices use a lot of power and aren't reliable enough for long-term. The conventional device has low slew rate, high power consumption, and nonlinear characteristics; however, due to zero static power, less load capacitance on input signals, faster switching, less transistors, and higher circuit density in this novel design, the device has a better slew rate and piecewise linear characteristics, and is seen consuming very low power in the order of 0.004mW. The Maximum Gain of 14 dB at 2 .3 GHz is obtained for a given circuit. Noise figure of the device is obtained as 0.24dB at 2.3-2.5 GHz range. The proposed circuit uses less total power per cycle, improves operation speed, is reasonably linear, and is easy to implement.**

Keywords — LNA, low power, simulation, Pseudo-PMOS, gain, noise factor, slew rate

I. INTRODUCTION

In almost all wireless communication systems, the Low Noise Amplifier is a critical factor. It is important for reducing the amount of noise in the signal received from the antenna [1]. The gain of this amplifier is also crucial since it lowers the noise figure of subsequent levels [2]. Friis' formula mathematically illustrates this principle as follows:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots . G_{n-1}}$$

Where, F_{total} denotes the system's total noise figure, n the number of stages, and G the stage's gain [3][4]. Wireless receiver's operating in the GHz range would benefit greatly from the proposed design.

Amplifier, input matching network, and output matching network are the three key stages of the basic LNA architecture. Figure 1 illustrates this. Stability, low noise figure, and high gain are all features of this amplifier [5][6]. Maximum power transfer is ensured by the input and output matching networks.

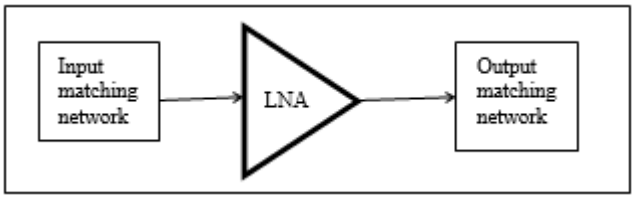

Fig. 1 Basic LNA architecture

To design LNA, extensive research and a variety of approaches have been suggested. Inductor, filter, common gate based Distributed amplifiers and shunt resistor based feedback amplifiers are some of the techniques widely used to achieve wideband input matching for LNA [7][8][9]. However, these techniques can have a number of drawbacks, including a large chip area, high power consumption, and insufficient NF[10].

This research paper describes a new pseudo PMOS-based inductor less LNA design that aims for small size, low static power and small size with significant gain. In order to achieve all mentioned above a novel Pseudo PMOS integrated low power inductor less LNA for wireless receiver with adequate voltage gain, and high linearity, with noise cancelling techniques (shunt feedback) is used in this proposed design.

II. CONVENTIONAL LNA

In general, feedback is a popular technique used in the design of wideband amplifiers to achieve input matching. LNA can achieve a very wideband (from 0-22 GHz) with less power consumed also significant high gain using resistive feedback [11][12]. The approach uses negative feedback and has limit to lower amplifier's input resistance and increase its bandwidth by lowering the tradeoff gain[13] [14]. In comparison to other techniques, resistive feedback LNAs configuration can achieve a smaller chip area since no or less inductors are added and utilized[15][16].

Noise cancellation technique is used to create noises with opposite polarities in the different paths and cancel out

 DOI : 10.35291/2454-9150.2021.0107

each other at the output. This method used for noise cancellation as well as impedance matching. Figure 2 demonstrates a noise cancelling technique-based simplified resistive shunt feedback LNA. This LNA is made up of a transistor M1, an RF resistor, and a gain of AX (AX>0) feed forward voltage amplifier [17]. The input impedance Zin is designed to fit the source impedance Rs for optimum power transfer [18].

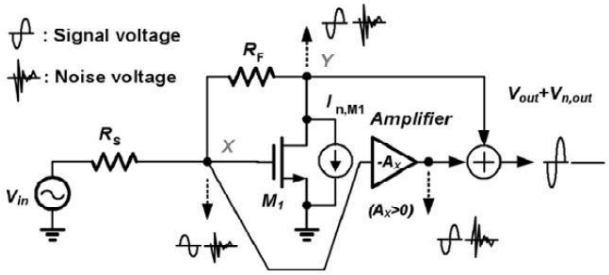

Fig. 2 Noise cancellation technique

III. PSEUDO PMOS

Pseudo-PMOS logic is a ratioed logic that realizes the logic feature by using a grounded PMOS as a load for pull-up network and Driver circuit is made up of NMOS pull-down network[19][20].

This logic is very important and low component count as it only uses N+1 MOSFETs as compared with 2N MOSFETs used in CMOS technology. Another merit of these type of circuits are that It has less load capacitance and fast switching as compared with another technologies [21] . The high output voltage level for any gate in pseudo-NMOS logic is VDD. As the VDD and ground has direct path through the PMOS transistor, the only major disadvantage of this logic is its extremely high static power consumption [22] [23].

IV. CIRCUIT DESCRIPTION

As shown in Fig.3, the proposed Pseudo PMOS inductorless LNA uses a resistive feedback topology for noise cancellation and output buffer levels. The input is connected by R_S, which has a source impedance of 50 ohm. R_{F1} is a shunt feedback resistor in the noise cancelling stage that is used for wideband wireless receivers for detecting the signal and noise of the input MOSFETs M_1, M_2 and M_3 to integrate the signal and deduct the noise of M_1. The load resistors R_{D1} and R_{D2} are being used to subtract the noise at M_2's drain, the signal polarities at M_1 and M_2's drains must be in phase.

The source follower is often used in wireless amplifiers to achieve wideband output matching. Source followers, on the other hand, have poor driving capacity and use a lot of voltage headroom in low voltage applications. In this novel design LNA is made up of M_4, R_{F2}, and R_{D4} and uses a resistive shunt feedback output stage further the circuit is built using a pseudo-PMOS technology which contains grounded gate PMOS . One NMOS is located just above the PMOS as mentioned will act as a switch, ON only when input is applied otherwise OFF. Hence, preventing the circuit from static power dissipation. The circuit diagram of proposed design is given in Figure. 3

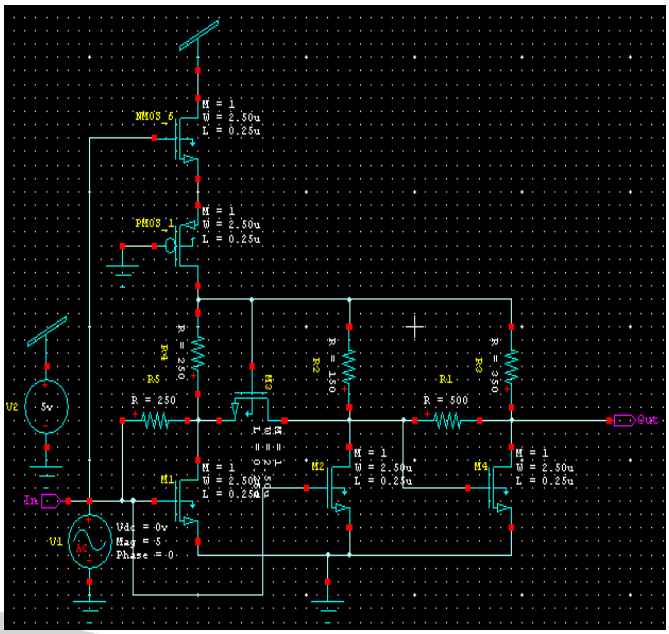

Fig. 3 Pseudo PMOS based LNA

The transient analysis is shown in Fig.4. Input signal shows linear variation with time as depicted by yellow

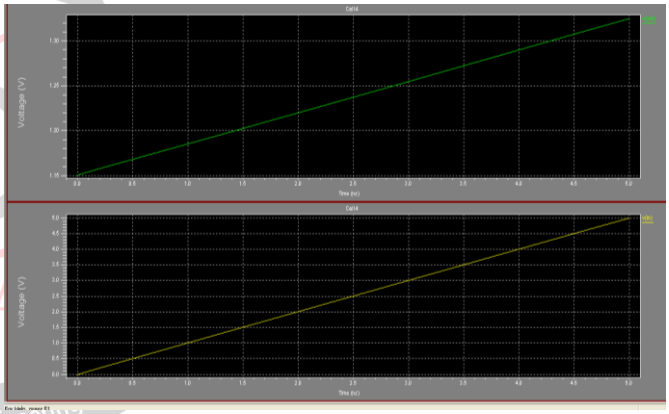

Fig. 4 Transient analysis of the device

graph. Similarly output also varies linearly with the input variation (indicated by the green graph). This shows that device is reasonably linear.

The parameters used to design the circuit is given in the Table 1 also the variation of voltage gain at different frequencies and at different levels are tabulated in the Table 2

Table: 1 Parameter description

Parameters	Values
R_{F1}	250Ω
R_{F2}	500 Ω
R_{D1}	250 Ω
R_{D2}	150 Ω
R_{D4}	350 Ω

 DOI : 10.35291/2454-9150.2021.0107

Table 2 Voltage and Gain variations

Voltage level	2.3GHz	3.1GHz	5.1GHZ	10GHz
1.4	2.8	2.7	2.3	1.2
1.6	3.9	3.8	3.5	2.4
1.8	5	4.8	4.5	3.4
2.3	5.9	5.8	5.4	4.3
3.3	9.4	9.3	8.9	7.8
4.3	11.8	11.6	10.9	10.2
5.0	14	13.8	13.3	12.2

The data presented above is represented graphically in Figure 5

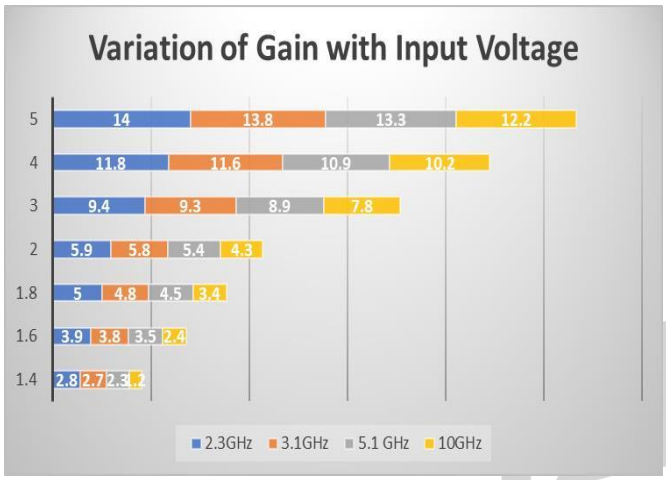

Fig. 5 Graphical representation of Table 2

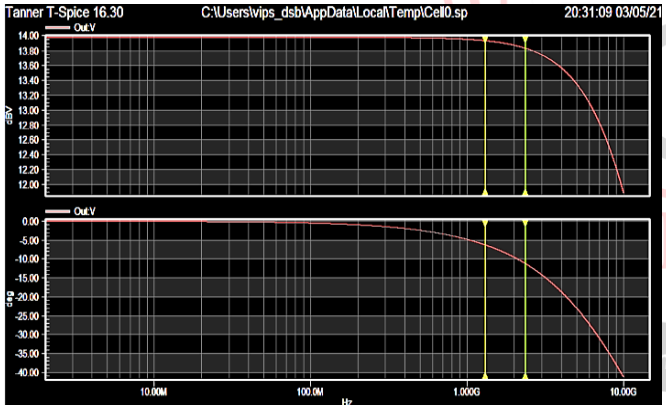

Fig. 6 AC analysis of the proposed circuit

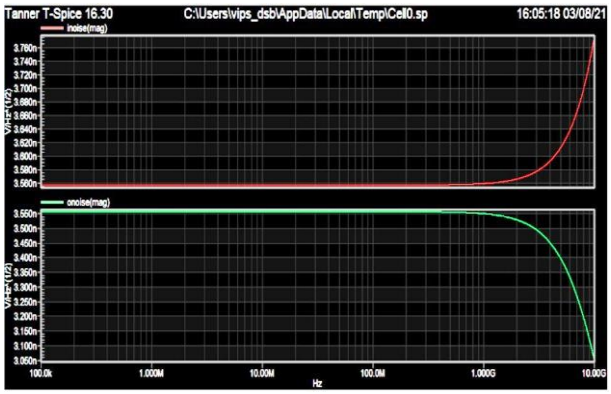

Fig. 7 Noise analysis of the given circuit

Table 3 Comparison with existing divces

[Ref]	Power (mW)	Gain (dB)	N.F (dB)	F0 (GHz)
[6]	30	22	3.5	1.5
[7]	12	22	2.5	2.5
[8]	22.4	19.8	3	2.4
[9]	7.2	15	2.2	2.4
[10]	4.5	13.4	3	2.5
[11]	-	15.9	2.88	2.45
[12]	13.2	11	2.2	2.4
[13]	7.33	20.34	1.98	2.4-2.5
[14]	4.49	26.48	1.044	2.45
Proposed design	0.004	14	0.24	2.4-2.5GHz

Comparison of the different parameters of LNA with the existing design has been done and presented in the Table 3 and its comparisons are also shown in Figure 8 and figure 9. From the parameters shown above it is inference that the proposed design consumes very less power in order of 0.004mW which is almost negligible as compared to other designs with a moderate gain of 14 dB with a NF of 0.24dB which is 1% as compared to the conventional designs in the range of 2.4- 2.5 GHz the ac analysis and the noise analysis of the device is shown in Figure 6 and Figure7.

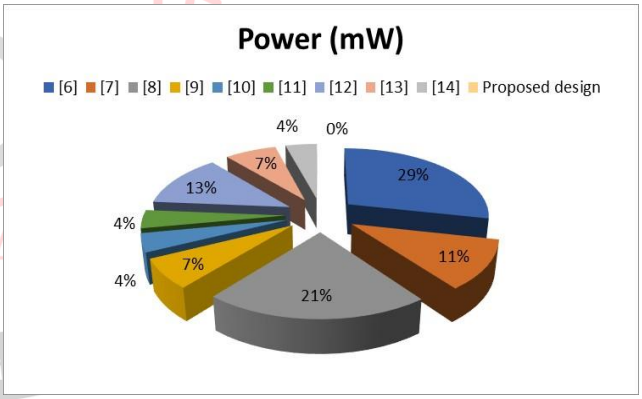

Fig. 8 Power consumption comparison w.r.t conventional device

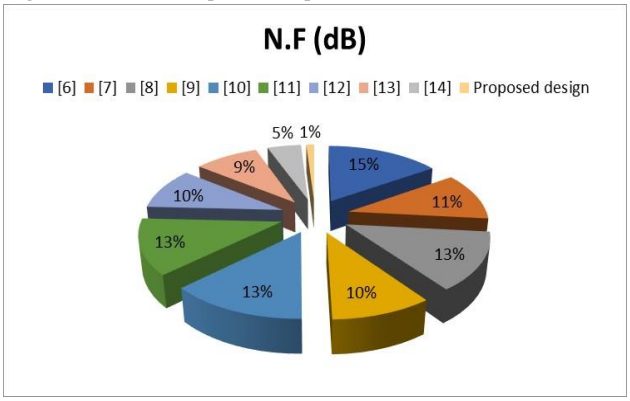

Fig. 9 Noise figure Comparison w.r.t conventional devices

V. RESULT

Proposed pseudo PMOS LNA design simulation are carried out in Tanner Tool of Mentor Graphics using 0.35 µm CMOS process technology. This section summarizes the

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different findings obtained. When we compare the latest design to the old design, we get the following findings.

(a) The number of MOSFETs in traditional devices is 10 in [1], 8 in [2], but only 6 in the latest model. As a result, major part savings are realized, resulting in cost savings.

(b) Static power is nearly zero. And the average power consumption obtain through the simulation is 0.004mW and the is included in the Appendix as a reference

(c) The new approach does not use a capacitor.

(d) In the traditional system, there are 4-3 current sources deployed, while in the modern device, there are none.

(e) The simulation of the circuit is carried out for different input voltage levels for wireless receivers and it has been found that for a particular voltage the gain gradually decreases as frequency increases from 1GHz to 10GHz.

(f) Also it is observed that the Max Gain of 14 dB at 2.3 GHz for input voltage of 5Vwhich gradually decrease to 13.8 at 3GHz and 13.2 to 5GHz and minimum 12.2 at 10GHz. This shows the Voltage gain decreases gradually when operating in a high frequency which may be due to intervening of parasitic capacitance at high frequency.

(g) The Noise figure for the simulated circuit is obtained as 0.24dB at 2.3 GHz

VI. CONCLUSION

A new Pseudo PMOS based LNA is proposed in this paper. The conventional device has low slew rate, high power consumption, and nonlinear characteristics; however, due to zero static power, less load capacitance on input signals, faster switching, less transistors, and higher circuit density in this novel design, the device has a better slew rate and piecewise linear characteristics, and is seen consuming very low power. Excellence of the method has been proven by computer simulations findings and comparisons with test data and simulations at transistor level. The analytical analysis is in line with all the findings.

VII. FUTURE SCOPE

A new system based on PP-LNA is proposed in this novel design. The PP that was implemented is a useful building block that simplifies the design of linear analogue systems. It also uses a small amount of energy. The slew rate has seen a noticeable change. The observed production is extremely linear. The proposed design's straightforward architecture and low component count are significant advantages. As a result, it's ideal for a wide-band wireless receiver. This research could be expanded to include additional changes in terms of power and scale, as well as wiring and layout characteristics.

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Power Results
vdd from time 0 to 5e-007
Average power consumed -> 4.142440e- 006 watts
Max power 3.061053e-005 at time 4.04571e-007
Min power 3.143356e-011 at time 1.05483e-007

Setup	0.01
seconds	
Transient Analysis	0.48
seconds	
Overhead	0.65
seconds	
Total	1.15
Seconds	

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