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Energy Efficient Reversible Binary to Gray Code Converter for Nanotechnology Application using Quantum Dot Cellular Automata (QCA)

[1]Preeti Das, [2]Anasuya Sikdar, [3]Dr. Prof. Sankit Ramkrishna Kassa

[1,2]Student, [3]Professor, Usha Mittal Institute of Technology, Mumbai, India, 1

[1]preetidas98@gmail.com, [2]anasuyasikdar04@gmail.com, [3]kassasankit@gmail.com

Abstract: As per Moore's law states the number of transistors get double every 18 months. The International Technology Roadmap for Semiconductors (ITRS) state that CMOS technology scaling will carry on till 2030. Consequences like oxide thickness, leakage current, electron migration, power dissipation, in feature size reduction are faced by the present transistor-based technology. The problem of interconnecting wires is solved by the QCA technology as coupling mechanism is done by Columbic interaction. Quantum Cellular Automata (QCA) is a new nanotechnology that has become one of the top six emerging technologies with an application potential to build future computers. The paper attempts to design a promising architecture which can employ quantum dots for digital computation to improve the efficiency of code converters.

Keywords—computation, coupling, electron migration, Moore's Law, nanotechnology, QCA, transistors

I. INTRODUCTION

In 1993, C.S Lent et. al. introduced the concept of Quantum dot cellular automation (QCA) which is an evolving, propitious, future generation nano-electronic computational architecture that encodes binary data/information as an electronic charge configuration of the QCA cell. It has the ability to evolve digital circuits with higher packaging density, minimized area, considerably low power dissipation, and higher switching speed. As it works at nanometer scale, QCA results in high-performance, ultra-dense digital devices.

II. BASICS OF QCA TECHNOLOGY

A. *QCA Cell*

A quantum cell is described as a square cell containing four quantum dots or quantum wells placed at its four corners. Two excess electronic charges are present in each cell which are localized in the dots only. These excess electrons repel each other when the cell is charged. These charges reside at the extreme corner of one of the diagonals of the square in order to attain maximum distance between them. Tunneling phenomenon is used by the cells to change their states which can happen by changing the position of individual electrons. Cell states are known as polarized with polarization represented by P. 'P = -1' indicates logic "0" and 'P = +1' indicates logic "1" (See Fig.1.). QCA cell is the main basic component of a QCA circuit. Various elements can be constructed using these QCA cells and can be used for implementation of larger complex circuits. [1]

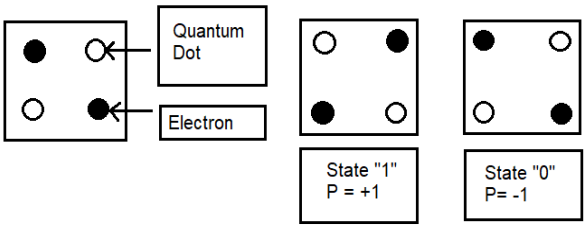

Fig. 1. QCA cell

B. *QCA Majority Gate*

The most fascinating feature of QCA Technology is the QCA Majority Gate. The Majority Gate works according to the following phenomenon where the input state which is in majority becomes the state of the output cell (See Fig.2.) The logical equation for a majority gate is as follows: F (A, B, C) =AB+AC+BC [1]

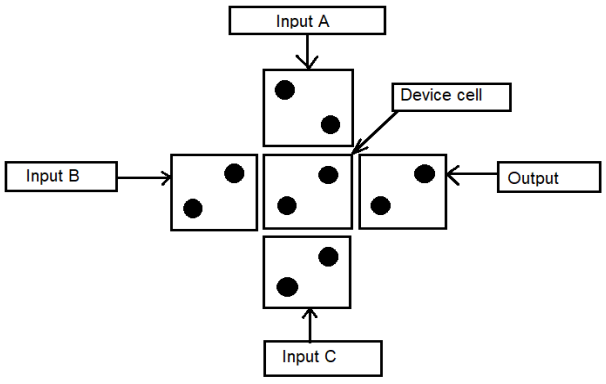

Fig. 2. QCA Majority Gate

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C. QCA Inverter, AND Gate and OR Gate

QCA inverter is generally composed by placing the cells with only their edges in contact. The reversed value of the input value is returned by the QCA inverter (See Fig.3.)

Implementation of the digital circuits can be done with the help of majority gate-based design techniques. Logical AND gate and OR gate can be implemented with the help of majority gate as shown in the following diagram (See Fig.4.)

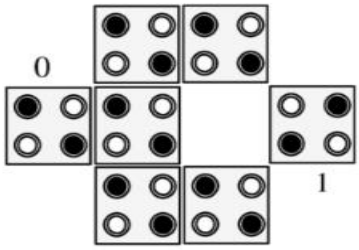

Fig. 3. QCA Inverter

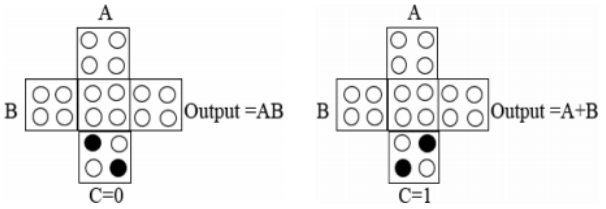

Fig. 4. QCA AND Gate and OR Gate

D. QCA Wiring

QCA wire is a package of interconnecting cells that are used to convey polarization state. QCA wire can be made up of 45º cells or 90º cells. The formal placement of QCA cells designs a binary wire. The signal promulgates from one end to another end of the cells for the need of electrostatic transmission. In a 45o QCA wire, the promulgation of the signal must be toggling between the two polarization. Both the arrangements are shown in the following diagram. (See Fig.5.)

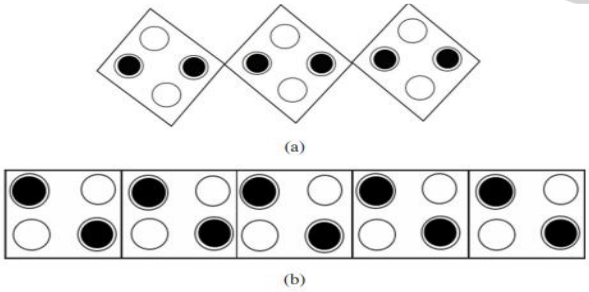

Fig. 5. QCA Wiring (a)45º (b)90º

E. QCA Clocking

QCA circuit requires a clock signal for the flow of information. The charge carrier punches the barrier instead of climbing through it and this phenomenon is known as Tunneling. QCA clocking consists of four distinct and periodic phases. The tunneling barrier tends to rise in the first phase or in the 'switch' phase. The second phase is the 'hold' phase wherein the barrier is quite high that no electron is able to tunnel through it. In the third phase or in the 'release' phase the barrier tends to lower down. And finally, in the ending phase or in the 'relax' phase the electron is able to tunnel. Clock energy is required to elevate or drop down the tunneling barrier which issues mandatory change in the circuit (See Fig.6.) [1]

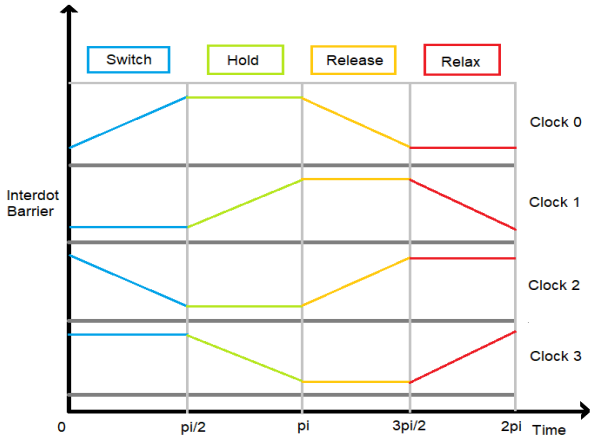

Fig. 6. QCA Clocking

III. BINARY TO GRAY CODE CONVERTER

A binary to gray code converter is a logical circuit which transforms the binary code to corresponding gray code.

The binary number system ordering of returned binary code or gray code is such that two consecutive values differ in only one bit (binary bit). Gray codes are very advantageous in the normal sequence of binary numerals produced by the hardware that may cause an obscurity or error during the transaction from one number to the next. Gray code can annihilate the problem quite easily because only one bit switches its value during any transition between two numbers.

A binary code is an illustrative presentation of data or text, instructions of a computer processor using a two symbol (number 0 and 1) system. For example, the decimal number 52 is equivalent to the binary sequence of six bits 110100.

Gray code is an ordering of the binary number system wherein each incremental value differs by one bit only. Gray codes are also called as Reflected Binary Code (RBC) or Cyclic Codes. While traversing from one step to another step of the Gray Code only one bit in the code group changes. Two adjoining code numbers vary from each other by only one bit.[7]

A. Steps to Convert Binary to Gray Code

The First bit of the given binary number corresponds to the Most Significant Bit (MSB) of the gray code and are exactly identical. The exclusive-or (XOR) of the First and Second bit of the given binary number corresponds to the second bit of the code. The third bit of gray code is equal to the exclusive or (XOR) of the second and third bit of the

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binary number. Thus, conversion from binary to gray code carries on. (See Fig.7.)

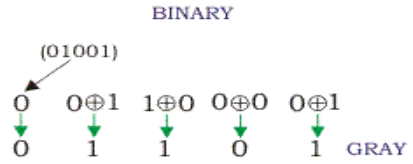

Fig. 7. Step Representation

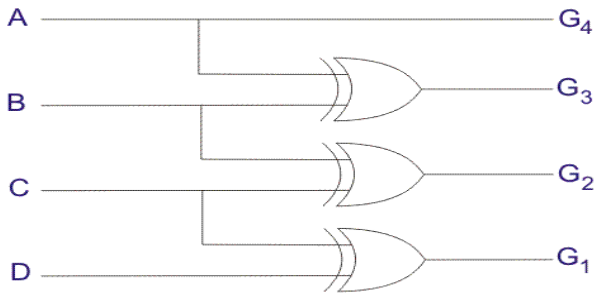

Fig. 8. Logical Circuit for Binary to Gray Code Converter

IV. REVERSIBLE BINARY TO GRAY CODE CONVERTER

A. *Feynman Logic Gate*

Feynman gate is a 2 x 2 reversible gate which is also called as controlled NOT gate (CNOT). The output vector O (P, Q) comprises of the input vector I (A, B) mapped into it. The correlation between the inputs and the outputs is provided by

$$P = A \quad (1)$$

$$Q = A \text{ xor } B \quad (2)$$

From the given truth table (See Table I), we can see that when the input is A = 0 the output is Q = B. But when A = 1, the output Q obtained is a compliment of B. The block representation clearly explain the functioning of Feynman gate. (See Fig.9.) [5]

TABLE I FEYNMAN LOGIC CIRCUIT TRUTH TABLE

INPUTS		OUTPUTS	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

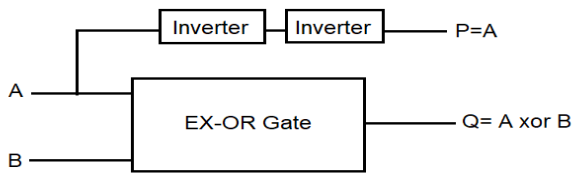

Fig. 9. Feynman Block Diagram

The Feynman gate is designed here is made with the help of three gates amongst which the two performs the NOT operation and one perform the EX-OR operation. The Feynman gate QCA circuit implementation and the simulation results are shown in the following figure. (See Fig.10. and Fig.11.)

This Proposed circuit contains of 33 QCA cell count, consuming 0.0106 μm^2 cell area and 0.06 μm^2 total area. This circuit provides a latency of 1.

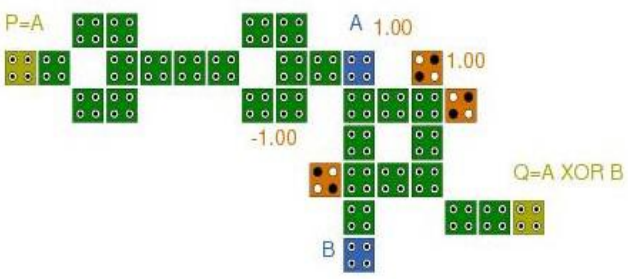

Fig. 10. Feynman Logic QCA Circuit

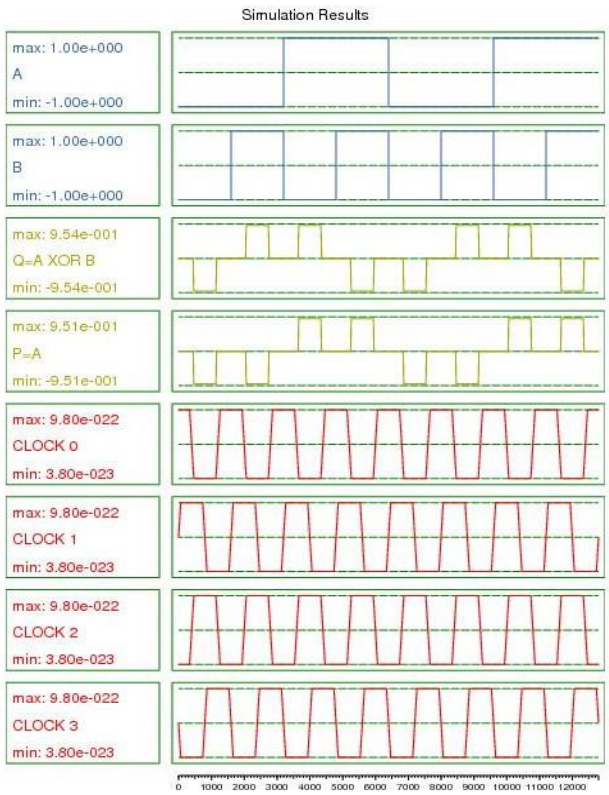

Fig. 11. Feynman Logic QCA Circuit Output

B. *3-bit Reversible Binary to Gray code converter using Feynman gate*

Considering a 3- bit reversible binary to gray code converter where I (A, B, C) is the binary input vector and O (P, Q, R) is the gray output vector. The block representation clearly explains the functioning of 3-bit Reversible Binary to Gray code converter using Feynman gate. (See Fig.12.) The truth table of 3- bit reversible binary to gray code converter is shown in Table No. II. From Table II, we can clearly state that the outputs follow

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the given equations:

$$P = A \quad (3)$$

$$Q = A \text{ xor } B \quad (4)$$

$$R = B \text{ xor } C \quad (5)$$

From the above equations, for implementing the 3- bit binary to gray converter we only need an EX-OR operation.

TABLE II 3-BIT REVERSIBLE BINARY TO GRAY CODE CONVERTER TRUTH TABLE

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

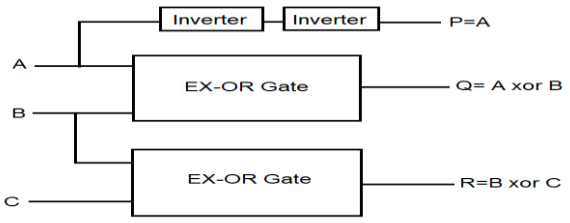

Fig. 12. Block Diagram of 3-bit reversible binary to gray code converter

Hence the prerequisite 3- bit converter can be executed by engaging two Feynman gates only as it creates least number of garbage outputs. The QCA 3- bit reversible binary to gray code converter using Feynman gate implementation and simulation results are as follows (See Fig .13. and Fig.14.) [2] [5]

This Proposed circuit contains of 50 QCA cell count, consuming 0.0162 μm^2 cell area and 0.10 μm^2 total area. This circuit provides a latency of 1.

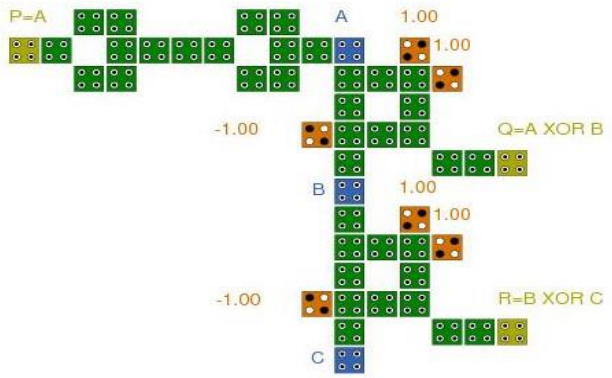

Fig. 13. 3-bit Reversible Binary to Gray code converter QCA Logic Circuit

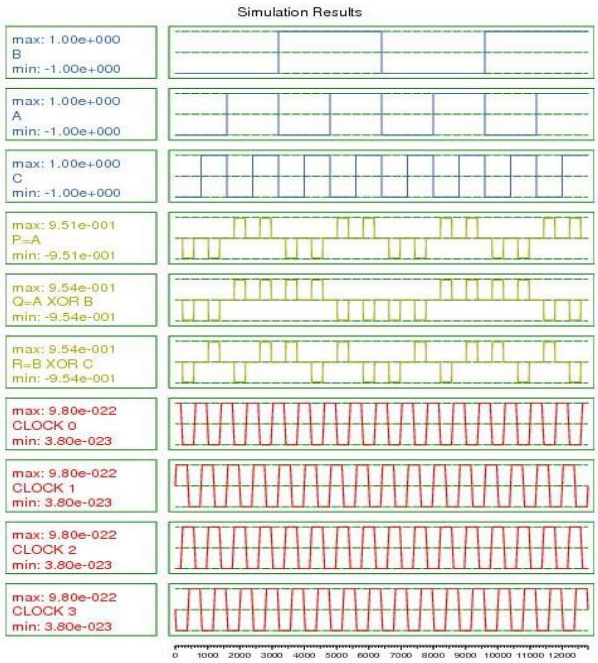

Fig. 14. 3-bit Reversible Binary to Gray code converter QCA Logic Output

C. 4-bit Reversible Binary to Gray code converter using Feynman gate

The Feynman gate is used as the basic building block to design the 4- bit reversible binary to gray code converter where I (A, B, C, D) is the input vector which is mapped into the output vector O (P, Q, R, S). The block representation clearly explains the functioning of 4-bit Reversible Binary to Gray code converter using Feynman gate. (See Fig.15.) The input output relationship for the 4-bit reversible binary to gray code converter is depicted in the following equations.

$$P = A \quad (6)$$

$$Q = A \text{ xor } B \quad (7)$$

$$R = B \text{ xor } C \quad (8)$$

$$S = C \text{ xor } D \quad (9)$$

From the equations it can be concluded that only ex-or gates are required for implementation of the given circuit. The 4- bit reversible binary to gray code converter truth table is given in Table III.

TABLE III 4-BIT REVERSIBLE BINARY TO GRAY CODE CONVERTER TRUTH TABLE

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0

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1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

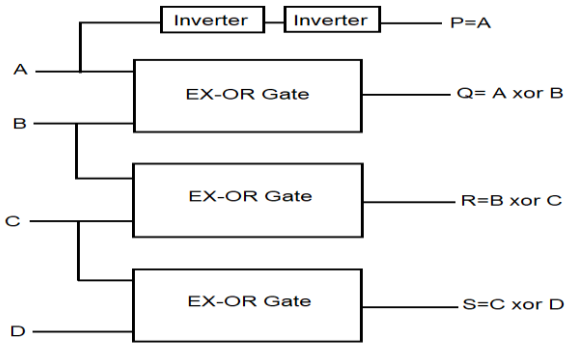

Fig. 15. Block Diagram of 4-bit Reversible Binary to Gray Code Converter

Thus, to design the 4- bit reversible code converter circuit only three Feynman gates are required. The 4-bit reversible binary to gray code converter using Feynman gate QCA implementation and the simulation result are shown in Fig. 16 and Fig.17. Because of modular approach attained by the design, there is a reduction in the complexity of the circuit. [2] [5]

This Proposed circuit contains of 67 QCA cell count, consuming 0.0217 μm^2 cell area and 0.15 μm^2 total area. This circuit provides a latency of 1.

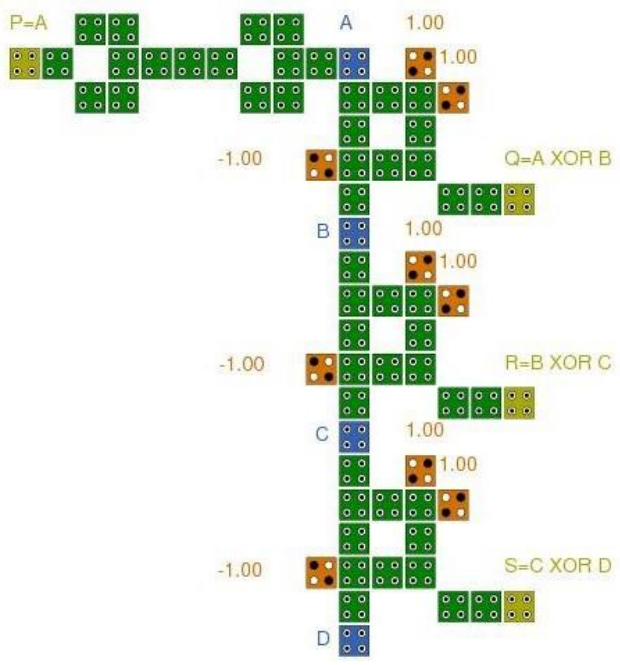

Fig. 16. 4-bit Reversible Binary to Gray code converter QCA Logic Circuit

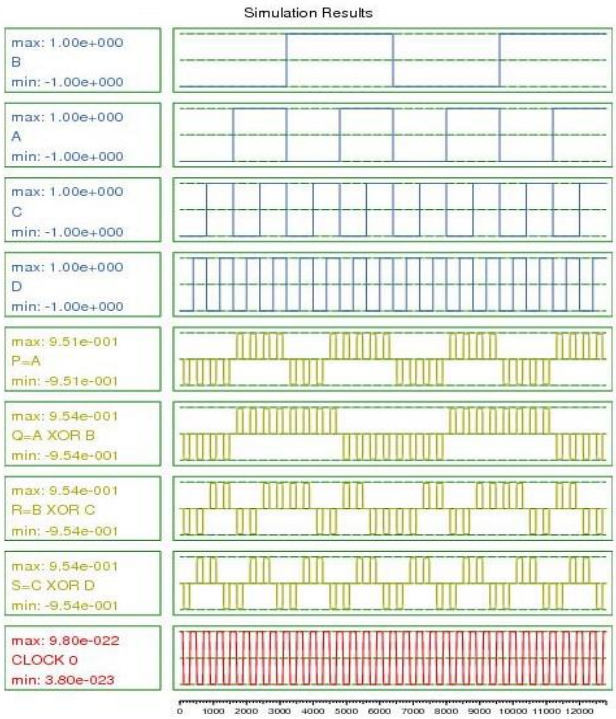

Fig. 17. 4-bit Reversible Binary to Gray code converter QCA Logic Output

V. RESULT

The paper attempts to design reversible code converter circuits using Quantum Dot Cellular Automata (QCA) Technology. Feynman Gate has been used as the fundamental block in the designing of reversible binary to gray code converters. From Table. IV it is evident that the proposed Feynman gate, 3-bit and 4-bit reversible Binary to Gray Code Converters are comparatively efficient in terms of cell count, cell area, total area, latency and complexity [5].

TABLE IV COMPARISON OF THE PROPOSED REVERSIBLE BINARY TO GRAY CODE CONVERTERS WITH PREVIOUS CODE CONVERTERS

Circuit	Cell Count	Cell Area (μm^2)	Total Area (μm^2)	Latency (in clock cycles)
3-bit Binary to Gray Code Converter (previous) [27]	59	0.0191	0.0622	0.75
3-bit Binary to Gray code converter (previous) [27]	61	0.019764	0.0771	0.75
4-Bit Binary to Gray Code Converter (previous) [1]	225	0.43	-	1
4-Bit Binary to Gray Code Converter (previous) [3]	389	0.13	0.69	8
Feynman Gate [5]	39	0.0126	0.07	4
3-bit reversible binary to gray code converter [5]	75	0.0243	0.13	4
4-bit reversible binary to gray code converter [5]	111	0.0359	0.20	4
Proposed Feynman Gate	33	0.0106	0.06	1
Proposed 3-bit reversible binary to gray code converter	50	0.0162	0.10	1
Proposed 4-bit reversible binary to gray code converter	67	0.0217	0.15	1

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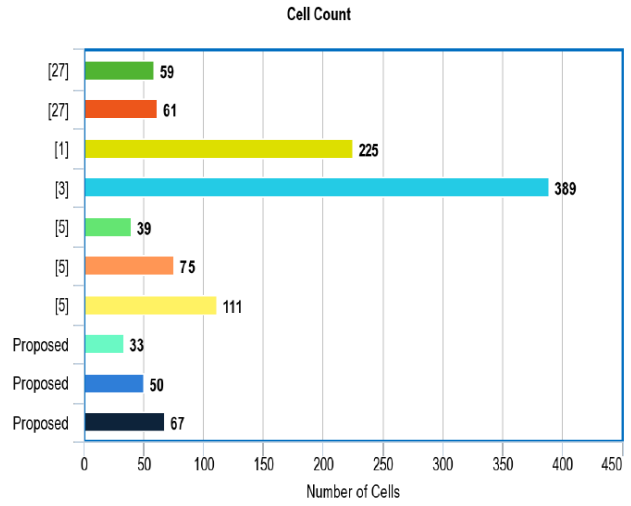

Fig. 18. Comparative Analysis: Cell Count

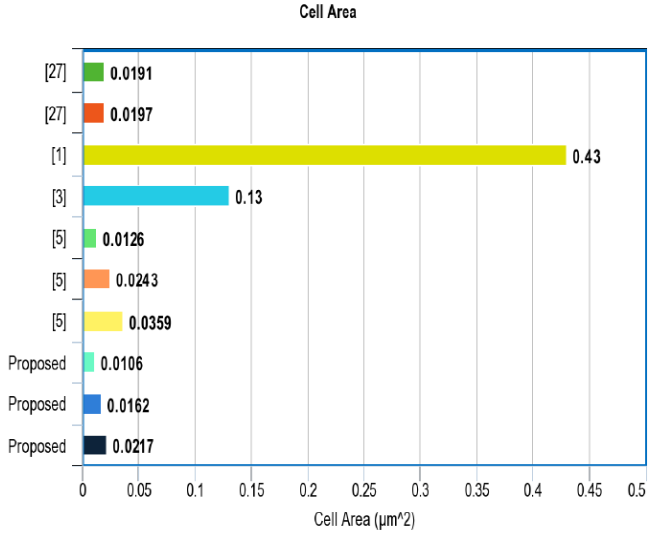

Fig. 19. Comparative Analysis: Cell Area

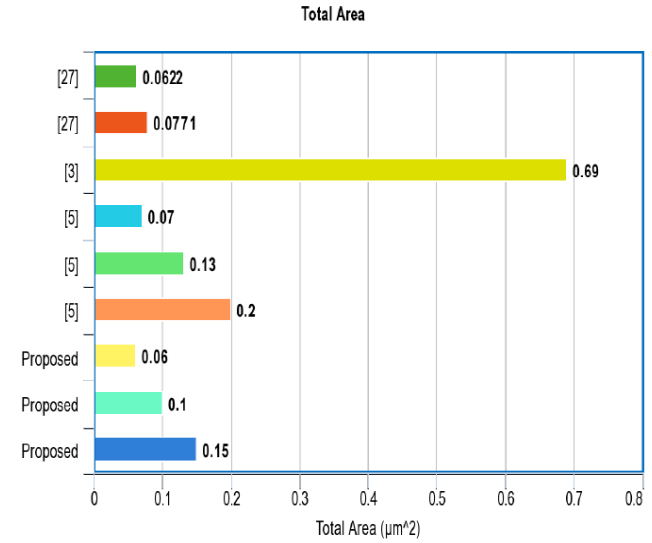

Fig. 20. Comparative Analysis: Total Area

VI. CONCLUSION

3-bit and 4-bit Reversible Binary to Gray Code converter using Feynman Gate was designed and implemented based on which the results were observed and determined. Comparing with previous research, the proposed code converter circuits use less cell count, total cell area and latency. As a result of which the circuits are energy efficient and can be used for various future digital computations.

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