Designing and Implementation of 1-bit Reversible Comparator in Quantum-dot Cellular Automata Nano-Technology

[1]Krutika Bhosale, [2]Rashmi Joshi, [3]Anuradha Patel, [4]Dr. Sankit Ramkrishna Kassa

[1,2,3]B. Tech Student, [4]Professor, ECE Department, Usha Mittal Institute of Technology, Mumbai, India, [1]krutikabhosale7127@gmail.com, [2]joshirashmi16@gmail.com, [3]aanei7123@gmail.com, [4]kassasankit@gmail.com

Abstract — Quantum-dot cellular automaton (QCA) an attractive, and emerging future generation nano electronic computational architecture. QCA technology is being suitable for low power digital circuits. It is a digital logical architecture which uses single electron in arrays of quantum dots to perform binary operations. The fundamental unit of the technology in building of QCA circuits is the QCA cell. A QCA cell, forms the base of every circuit which can be utilized to build basic gates and logic devices in QCA architectures. This paper evaluates the performance of implementations of QCA based reversible comparator using Feynman gate and proposes layouts with better performance parameters. The paper also explores an advance design of Feynman gate using QCA with reduced numbers of QCA cells. Quantum cost effective 1-bit reversible comparator circuit using Feynman gate is proposed. The designing of 1-bit reversible comparator and Feynman gate is made with the attempt to reduce cell count, delay and area as well. The simulation results show that the proposed circuits perform well. This paper helps to design area efficient higher complex circuit using reversible gate.

Keywords — Nanotechnology, Quantum-dot cellular automata, Reversible Comparator, Feynman gate

I. INTRODUCTION

Quantum-dot cellular automata (QCA) is an evolving nano-electronic technology that presents a revolutionary approach to computing at nano level. A thorough research and development in the field device technology for the past several years which lead to the availability for designers and processing engineers rapidly with frequently reducing size of the semiconductor devices and operating current. On the nanometer scale the constant development in device fabrication is finite by process technology and fundamental problems arising from scaling which includes quantum-mechanical effects, severe power dissipation and one of the critical issues in VLSI circuit. The tunneling current increases in MOS (Molecular Orbitals) circuits with the future size deteriorating to deep submicron device geometry process. The characteristics of design and circuit significantly are drifted from the designer's expectations of making improvements suited from application perspective. In several studies it is examined that these device technologies are approaching its physical limits. Two separate states can be utilized in any physical phenomenon to convey a logic variable in two valid logic states such as electronic spin. Quantum is a chosen effect to be used in representing logic rather than any other method. Quantum logic devices are explored under this consideration and one of it is known to be Quantum-dot Cellular Automata (QCA). It is an arising model or a prototype, allowing operating frequencies in the range of THz and device integration densities about 900 times than the current end of conventional complementary metal oxide semiconductor (CMOS) scaling limits. It has been stated as one of the emerging nanotechnologies in Semiconductor Industries Association's by International Technology Roadmap for Semiconductors (ITRS). QCA predicated circuits have an edge of high speed, high integrity and low power consumption. Add on QCA circuits have a benefit of high parallel processing. Also, QCA can achieve high density, fast switching speed, and room temperature operation [1].

The key parameters in designing digital logic circuit to perform nano-computing are heat energy dissipation and circuit density. The energy dissipation can be patched up using reversible logic circuits produced by irreversible logic circuits. If one bit of the information is lost it produces heat energy dissipation as kBTln2 joules, kB (Boltzmann's constant) and T (absolute computing temperature). In logic computing, very low heat dissipation can be achieved

 DOI : 10.35291/2454-9150.2021.0226

through reversible computing. Reversible logic circuit has wide spread versatility in nuclear magnetic resonance, quantum, and optical computing. QCA, a transistor-less technology, in which the columbic relation between QCA cells creates the path of propagation of information through QCA wire. In QCA, information is carried out depending on the charge of an electron that occupy within a QCA cell rather than electrical power like in CMOS circuits. The ultra-low power utilization of QCA circuit may have an arising functionality in reversible logic circuit design. This paper illustrates an optimized design of Feynman gate and reversible 1-bit comparator along with its implementation in QCA [1] [2].

II. QCA FUNDAMENTALS

The section below has briefly described the introductory of QCA and computation mechanism using QCA cells.

A. Basic QCA Cell

A QCA cell is a structure that consists of four quantum dots arranged in a square pattern as shown in **Figure (1).** These quantum-dots are the spaces in which electrons are able to reside and tunnel between them but cannot leave the cell [2].

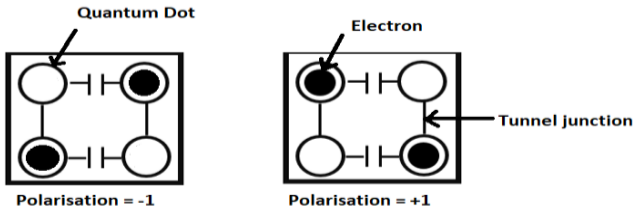


Figure 1. QCA cell and polarizations of QCA

In many identical QCA cells, information processing is based on the Columbic interactions between the cells. Each structure is built using four electronic sites or dots coupled through quantum mechanical tunneling barriers. The electronic sites represent those locations that a mobile electron can occupy. The cells contain two mobile electrons (or holes) which repel each other as a result of their mutual Columbic interaction in the ground state and tend to occupy the diagonal sites of the cell. Therefore, the cell has two degenerate ground states. This leads to two polarizations of a QCA cell, denoted as P = +1 and P = −1 respectively. Binary information can be encoded in the polarization of electrons in each QCA cell. Thus, logic 0 and logic 1 are encoded in polarization P = −1 and P = +1 respectively. **Figure (1)** also shows the two possible polarizations of a QCA cell. In these devices, binary computation requires interaction among bits. When a second cell is placed near the first cell, the coulomb interaction between the cells removes the degeneracy and determines the ground state of the QCA cell and polarizations of QCA cell **Figure (1) [Left]**. The interaction between the QCA cells is non-linear that is with a small perturbation from a neighboring cell that clicks it into essentially aligned configuration either with P = +1 or P = −1 so as appropriate.

Calculation method for the polarization in the QCA cell is shown in equation (1):

$$P = \frac{(p1 + p3) - (p2 + p4)}{p1 + p2 + p3 + p4} \quad (1)$$

B. QCA wires

A QCA wire is nothing but a line of QCA cells. The QCA wire is driven at the input cell by another cell with a constant polarisation. Due to the electrostatic interactions between cells, the binary signal travels from input to the output of the QCA wire. The propagation in a 90˚ QCA wire is as shown in **Figure 2(a)** [3].

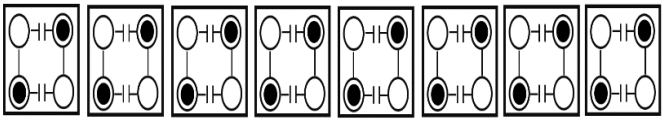


Figure 2(a). QCA wire (90˚)

And other than the 90˚ QCA wire, a 45˚ QCA wire can also be used but with different arrangement of the cells, that is rotating the cells with 45˚ as shown in the **Figure 2(b)**. The propagation of the binary signal alternates between the two polarizations of the cell.

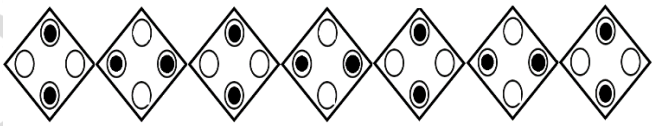


Figure 2(b). QCA wire (45˚)

C. QCA clock

In the QCA technology, the clock is utilized for information flow controlling. The QCA clock is divided into four phases. **Figure (3)** shows the clock zones in the QCA technology [4].

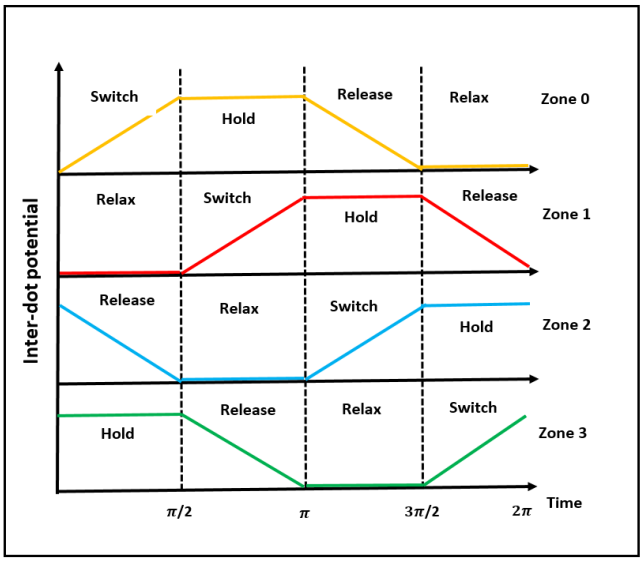


Figure 3. Clock zones in QCA technology

 DOI : 10.35291/2454-9150.2021.0226

As shown in **Figure (3)**, the depolarisation of the cells begins during the Switch phase. The potential barriers within the cells are low in the Switch phase. However, in hold phase the electrons cannot change their positions within the cell. Therefore, the barrier potential is gradually decreasing at the end of this phase. So, the cells begin to depolarize during the Release phase. When the barriers are at their lowest level, the clock phase changes to the Relax phase. Therefore, the cells remain in this state and the cell barriers stay at their lowest level.

D. QCA gate

A basic QCA logic gate is nothing but a majority gate.

The 3-input QCA majority gate is shown in **Figure (4).**

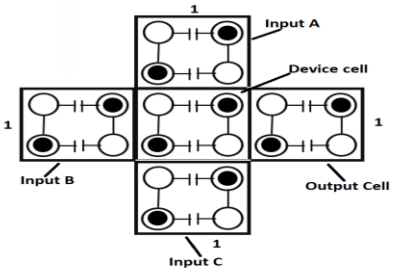


Figure 4. The 3-input QCA majority gate

The logical equation of the 3-input majority gate is defined as mentioned in the equation (2):

$$Maj(A, B, C) = AB + AC + BC \quad (2)$$

The majority gate is a logical gate which is being used in the complex QCA circuits. The output of the majority gate is considered as true provided more than 50% of its inputs is true. The inputs of the basic majority gate are taken as 3, 5, 7… (2n + 1) bits [2].

The logic of AND gate and OR gate is realized by fixing the polarization of either of the inputs of the majority gate to P = −1 (logic "0") or P = +1

(Logic "1") [5].

The layout and the logic circuit for the AND gate is shown in **Figure (5)**.

Figure 5(a). Logic circuit of AND gate

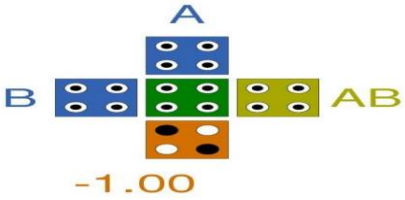


Figure 5(b). Implementation of AND gate in QCA

The layout and the logic circuit for the OR gate is shown in **Figure (6)**.

Figu B a). Logic circuit of OR gate

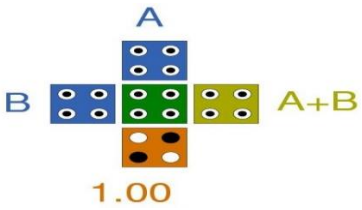


Figure 6(b). Implementation of OR gate in QCA

E. QCA Exclusive OR Implementations

In addition, with AND, OR gates and exclusive-OR (XOR) gates is also utilised in the design of digital circuits. Exclusive OR gates are provided with special functions and applications. These gates are especially useful in arithmetic operations as well as error detection. XOR gates usually consists of 2-input gates, as they are complex to fabricate with hardware and no multiple-input XOR gates are available [6] [7].

The exclusive-OR (XOR) performs the following logic operation as mentioned in the equation (3) [8] [9]:

$$A \oplus B = A'B + AB' \quad (3)$$

The truth table of XOR gate is shown in **Table (1)**.

A	B	A⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

Table 1: Truth table for XOR gate

The layout and the logic circuit for the XOR gate is shown in **Figure (7)** [10].

Figure 7(a). Logic circuit of XOR gate

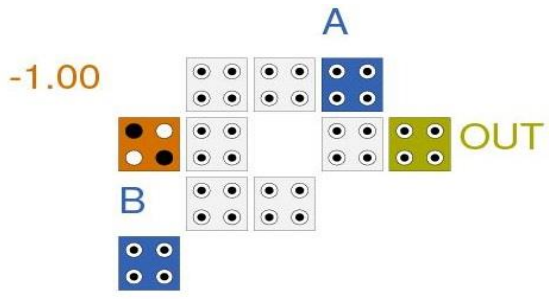


Figure 7(b). Implementation of XOR gate in QCA

 DOI : 10.35291/2454-9150.2021.0226

F. QCA Comparator

Comparators, a hardware electronic device that takes two integers in the binary form as inputs and determines whether one integer is greater than, less than or equal to another integer (A > B, A < B and A = B). The truth table for the 1-bit comparator is as shown in **Table (2)**. These are used in the CPUs as well as in microcontrollers [11] [12].

A	B	A < B	A = B	A > B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Table 2: Truth table for 1-bit comparator

From the truth table of 1-bit comparator, the logical equations for each output can be expressed as mentioned in equation (4), (5) and (6):

a) If A < B then $A\bar{B}$ **(4)**

b) If A = B then $A\bar{B} + \bar{A}B$ **(5)**

c) If A > B then AB **(6)**

The logic circuit for the 1-bit comparator is shown in **Figure (8)** [13] [14].

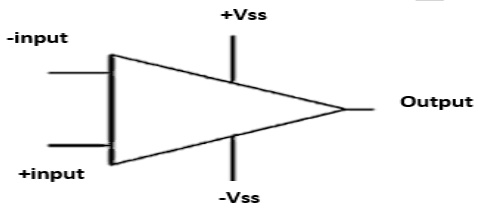


Figure 8. Logic circuit of the 1-bit comparator

III. Feynman Gate

Feynman gate is a 2*2 gate which is also known as controlled NOT and is widely used for fan-out purpose. Feynman gate is a reversible logic gate consisting of two inputs and their corresponding outputs. The input bits (A, B) have one-to-one mapping function to output bits (P, Q). It has quantum cost 1 [15].

The logic circuit and Truth table of proposed Feynman gate is shown in **Figure (9)** and **Table (3)**. The proposed Feynman gate using QCA cells is depicted in **Figure (10)** [16] [17].

The logical equations (7) (8) for outputs are given as,

P = A **(7)**

Q = $A \oplus B$ **(8)**

Input		Output	
A	**B**	**P**	**Q**
0	**0**	**0**	**0**
0	**1**	**0**	**1**
1	**0**	**1**	**1**
1	**1**	**1**	**0**

Table 3: Truth table of proposed Feynman gate

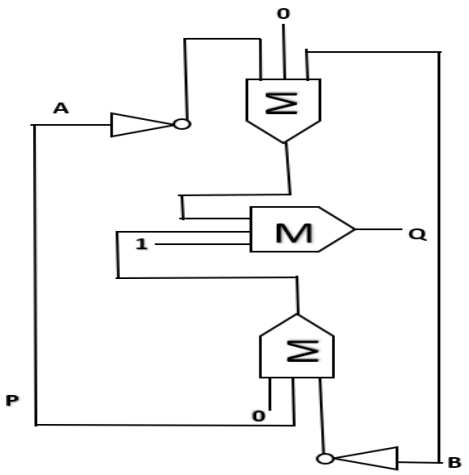


Figure 9. Logic circuit of Proposed Feynman gate

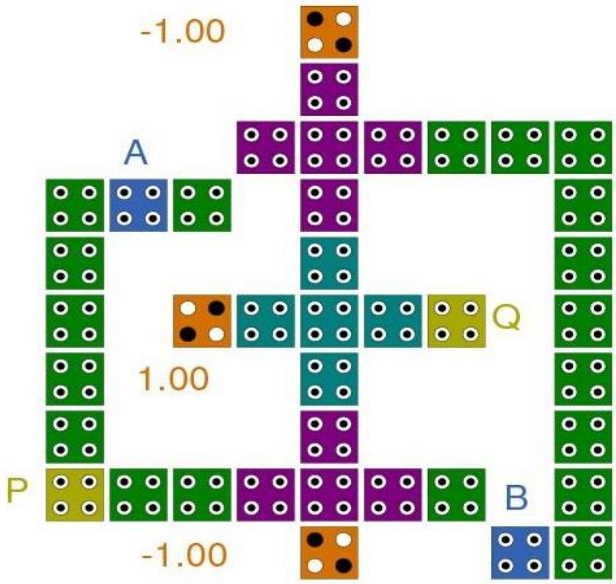


Figure 10. Implementation of Proposed Feynman gate

IV. Proposed QCA Comparator

Comparison is the most basic arithmetic operation that determines if one is greater than, equal to, or less than the other number. [18][19]

The Proposed 1-bit reversible comparator is designed using Feynman gate. The block representation and truth table of proposed reversible comparator is shown in **Figure (11)** and **Table (4)** [20] [21].

The proposed 1-bit reversible comparator using QCA cells is depicted in **Figure (12)**.

Input		Output		
A	**B**	**L**	**G**	**E**
0	**0**	**0**	**1**	**0**
0	**1**	**0**	**0**	**1**
1	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**

Table 4: Truth table of proposed reversible comparator

 DOI : 10.35291/2454-9150.2021.0226

The logical equations of the proposed reversible comparator can be expressed as shown in the equations (9), (10) and (11).

L=A<B **(9)**

E=A=B **(10)**

G=A>B **(11)**

Thus the logical expression of the circuit is given in the below equations (12), (13) and (14).

L = AB' **(12)**

E = A ⊙ B **(13)**

G = A'B **(14)**

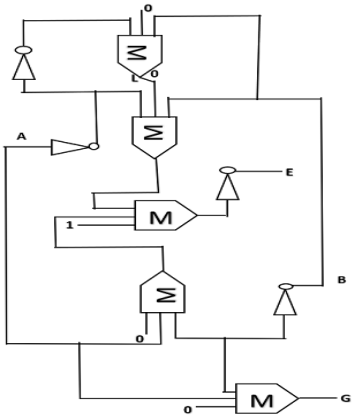


Figure 11. Logic circuit of 1-bit reversible comparator

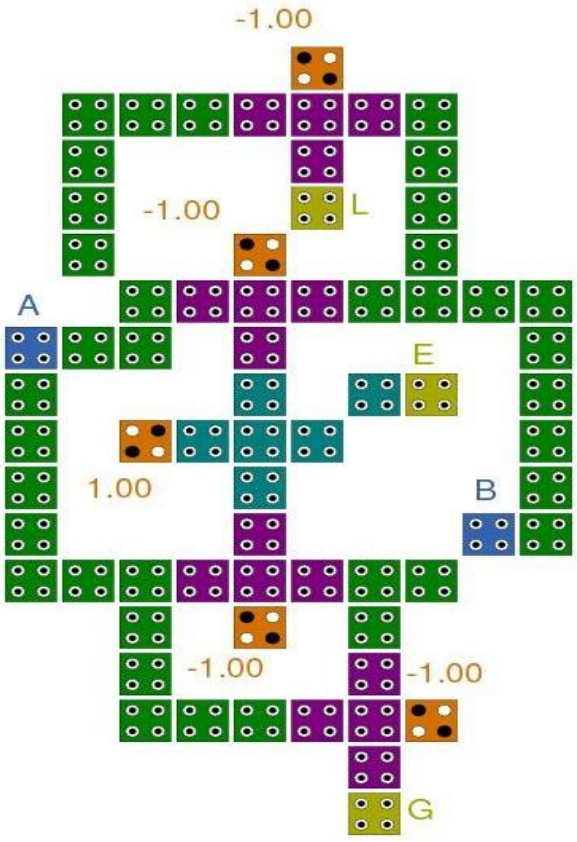


Figure 12. Implementation of 1-bit reversible comparator

V. Simulation Results and Comparisons

The comparison of the proposed QCA reversible comparator and Feynman gate circuit with the existing designs are analyzed in this section. The Design and simulation are achieved by using Bistable approximation and QCA tool 2.0.3 version. The list of parameters used for Bistable approximation are demonstrated in **Table (5)**.

The proposed reversible comparator and Feynman gate circuit are compared with the existing designs. The comparisons are shown in **Table (6)** and **Table (7)**. Cell count is the number of cells used for designing purpose. **Figure (13)** demonstrates the simulation output of Feynman gate. The result is verified theoretically prescribed in **Table (6)**.

Figure (14) demonstrates the simulation output of proposed reversible comparator. The result is verified theoretically prescribed in **Table (7).**

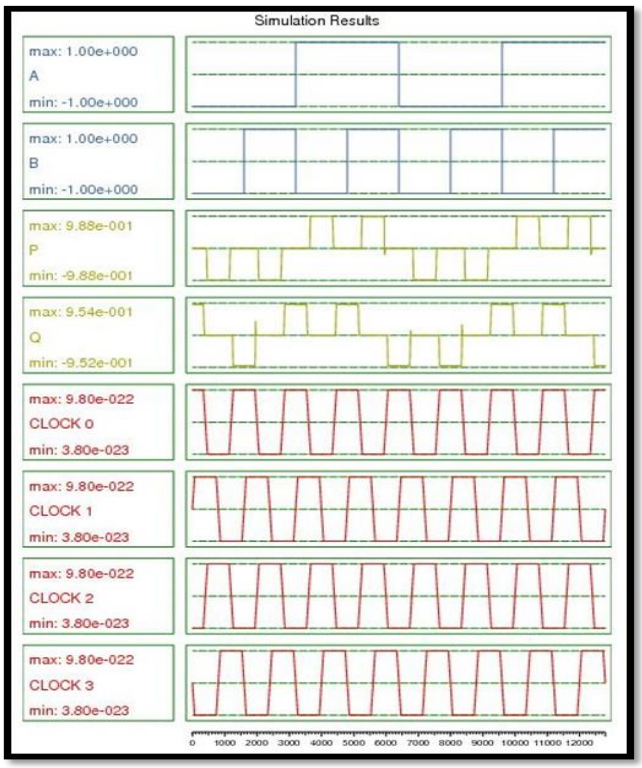


Figure 13. Simulation results of proposed Feynman gate

 DOI : 10.35291/2454-9150.2021.0226

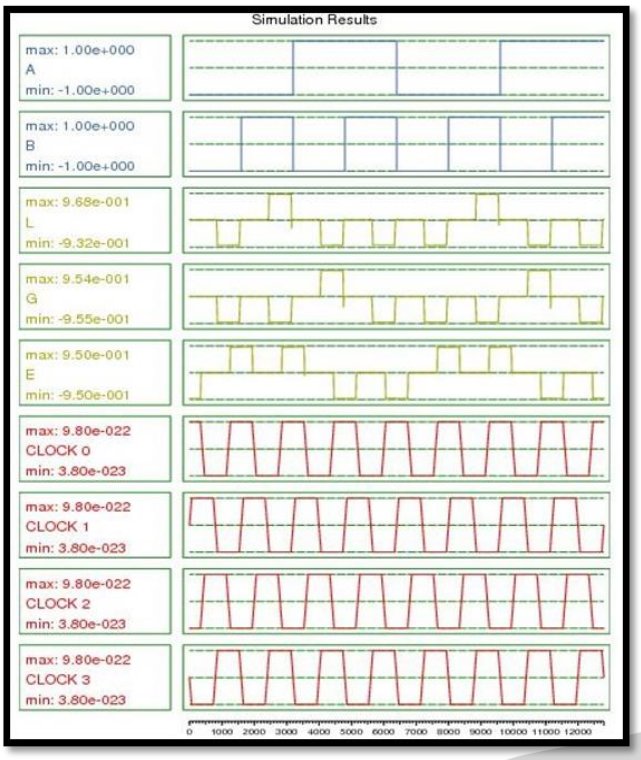


Figure 14. Simulation results of proposed reversible 1-bit comparator

Number of Samples	**12800**
Convergence Tolerance	**0.001000**
Radius of effect (nm)	**65.000000**
Relative Permittivity	**12.900000**
Clock High	**9.800000e-22**
Clock Low	**3.800000e-22**
Clock Shift	**0.000000e+000**
Clock Amplitude Factor	**2.000000**
Layer Separation	**11.500000**
Maximum Iteration Per Sample	**100**

Table 5. Simulation Parameters for Bistable Approximation

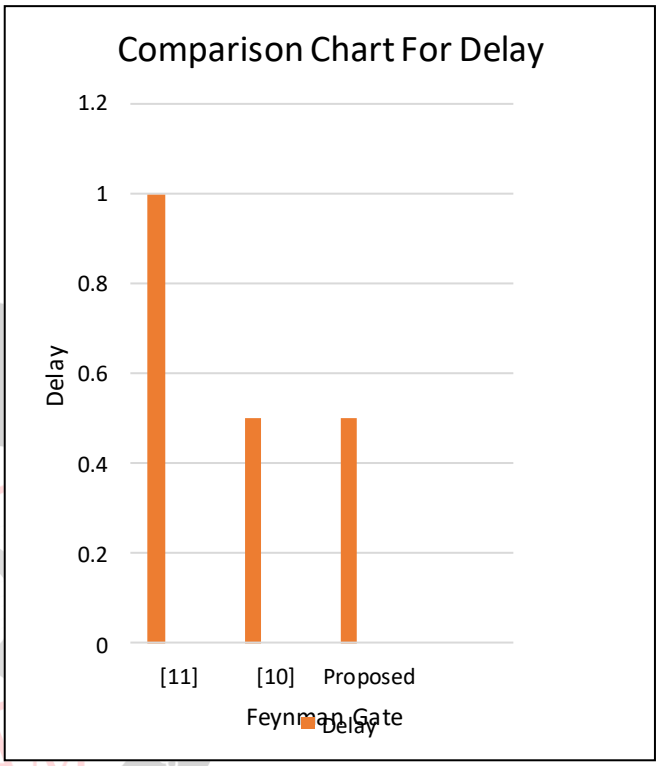
The result demonstrates that output of proposed 1-bit reversible comparator circuit and proposed Feynman gate are correctly obtained after 0.5 clock cycle delay. QCA cell count is the number of cells which are required to design 1-bit reversible comparator circuit and Feynman gate. All these designs have 18nm * 18 nm individual area. Therefore, minimum number of cell count are desirable for better area. Moreover, the designed 1-bit reversible comparator circuit requires 0.07 µm² area and 69 cells. Similarly, the proposed Feynman gate requires 0.04 µm² area and 40 cells.

Summary of simulation results of proposed 1-bit reversible comparator circuit and proposed Feynman gate which are compared with existing designs are demonstrated in **Table (6)** and **(7)** respectively.

Reference	Cell count	Area (µm²)	Delay (Clock cycle)
[11]	65	0.09	1
[10]	51	0.07	0.5
Proposed Design	40	0.04	0.5

Table 6. Comparison for Feynman Gate

Figure 15. Comparison Chart of Cell count of Feynman Gate



 DOI : 10.35291/2454-9150.2021.0226

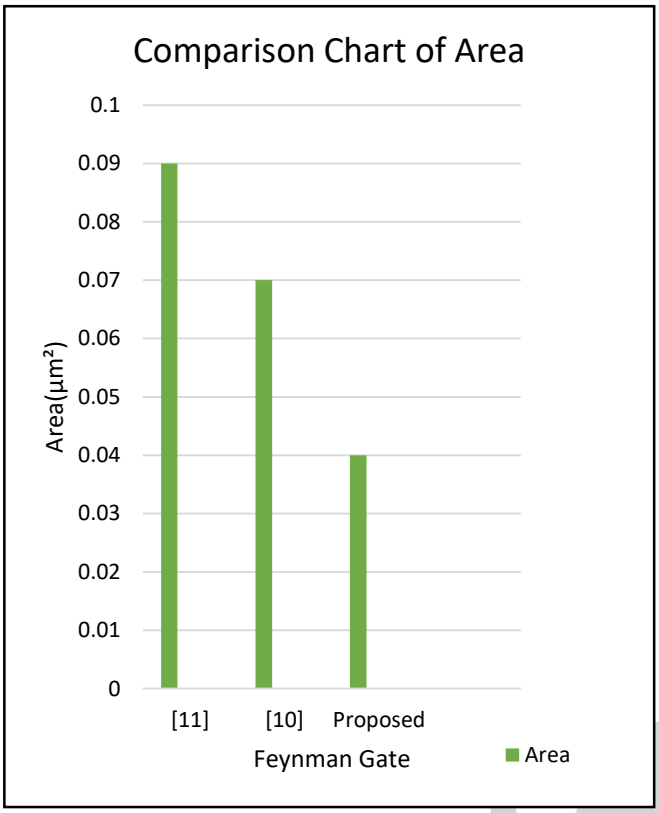


Figure 16. Comparison Chart of Area of Feynman Gate

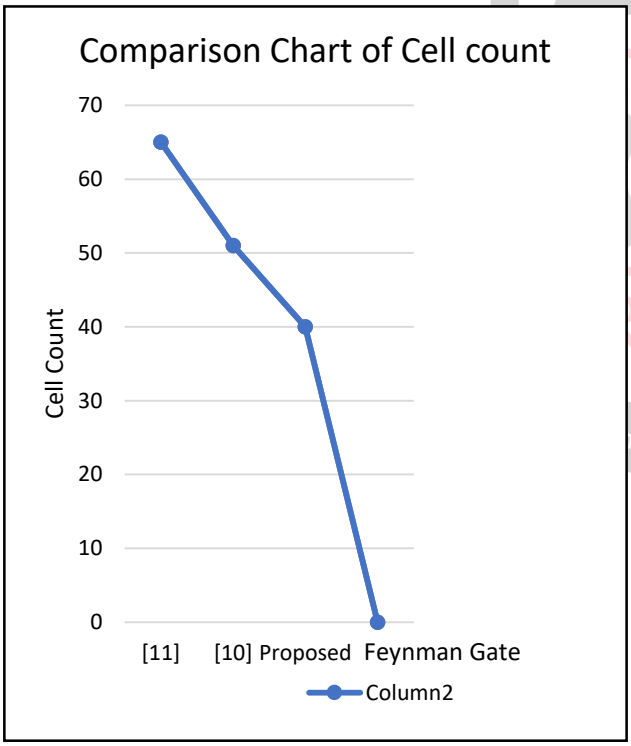


Figure 17. Comparison Chart for Delay of Feynman Gate

Reference	Cell count	Area (µm²)	Delay (Clock cycle)
[4]	319	0.343	3
[6]	223	0.21	2
[7]	220	0.23	0.75
[8]	117	0.182	1
[9]	97	0.14	1
[10]	87	0.11	0.5
Proposed Design	69	0.07	0.5

Table 7. Comparison for QCA 1-bit Comparator

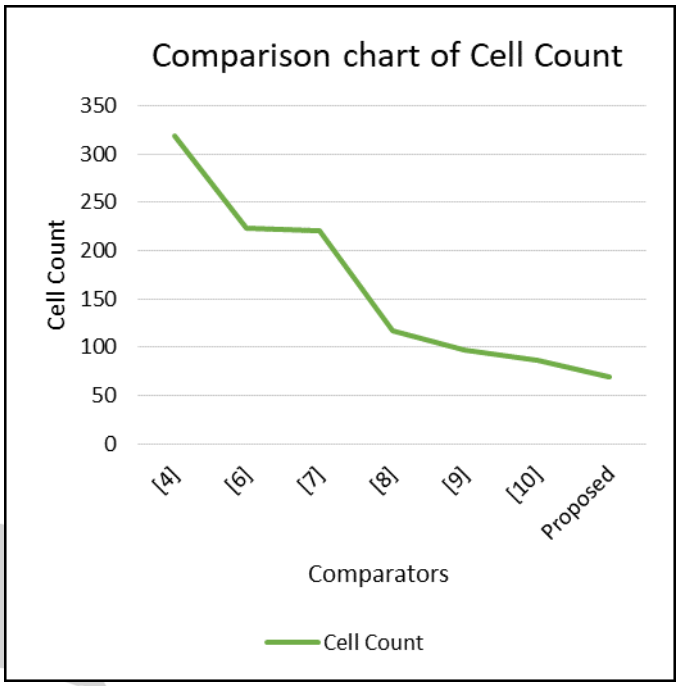


Figure 18. Comparison chart of Cell Count of Comparators

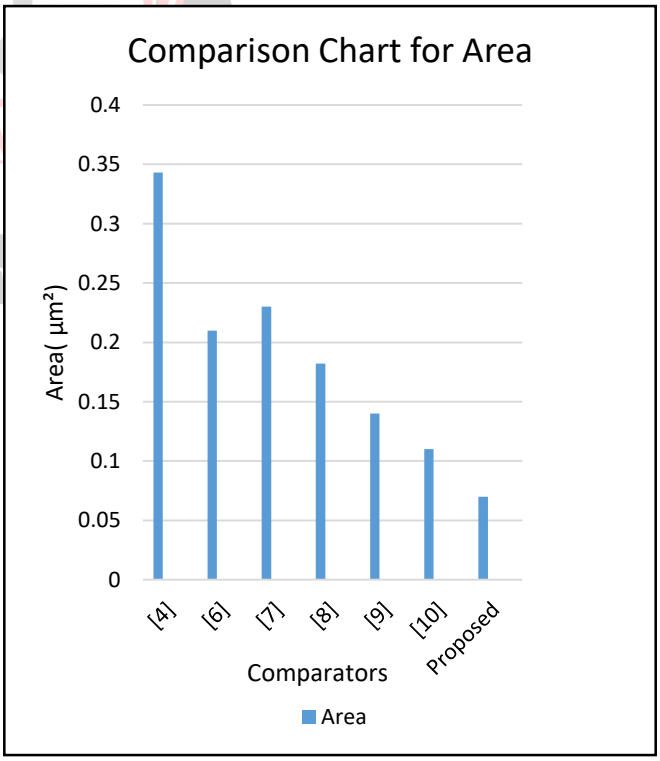


Figure 19. Comparison Chart for Area of Comparators

 DOI : 10.35291/2454-9150.2021.0226

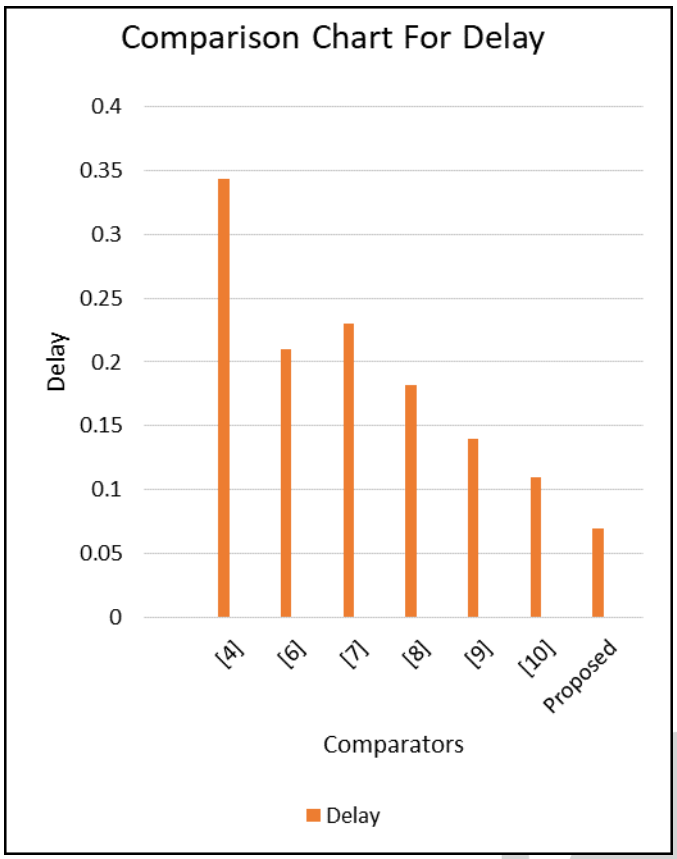


Figure 20. Comparison Chart for Delay of Comparators

VI. Conclusions

The QCA technology is an encouraging and co-operative technology for circuit design at nano scale. This paper explores an advance design of Feynman gate using QCA with reduced numbers of QCA cells. Quantum cost effective 1-bit reversible comparator circuit using Feynman gate is proposed. The performance of the proposed QCA reversible comparator and Feynman gate has been verified using QCADesigner tool version 2.0.3. CAD tool, a QCADesigner designed specifically for QCA logic design and simulation. During the designing of 1-bit reversible comparator and Feynman gate attention is made to reduce cell count, delay as well as area. The simulation results show that the proposed circuits perform well. This paper helps to design area efficient higher complex circuit using reversible gate. Hence, paper concludes that the proposed design should be a promising step towards the goal of achieving advancement in QCA nanotechnology.

VII. References

[1] J. C. Das and D. De, "Quantum Dot-Cellular Automata based cipher text design for nano-communication," 2012 International Conference on Radar, Communication and Computing (ICRCC), Tiruvannamalai, India, 2012, pp. 224-229

[2] K. Walus, G. Schulhof, G. A. Jullien, R. Zhang, and W. Wang, "Circuit design based on majority gates for applications with quantum-dot cellular automata," in Conf. Rec. 38th Asilomar Conf. Signals, Systems and Computers, 2004, vol. 2, pp. 1354–1357.

[3] Bahrepour, Davoud. (2015). A Novel Full Comparator Design Based on Quantum-Dot Cellular Automata. International Journal of Information and Electronics Engineering. 5. 10.7763/IJIEE. 2015.V5.568.

[4] Das, Jadav & De, Debashis. (2015). Reversible Comparator Design Using Quantum Dot-Cellular Automata. IETE Journal of Research. 62. 1-8. 10.1080/03772063.2015.1088407.

[5] Ali Hussien Majeed, Mohd Shamian Zainal, Esam Alkaldy, Danial Md. Nor, Single-bit Comparator in Quantum-dot Cellular Automata (QCA) Technology Using Novel QCA-XNOR Gates, Journal of Electronic Science and Technology,2020,100078, ISSN 1674-862X

[6] B. Lampreht et al., "Quantum-Dot Cellular Automata Serial Comparator," 2008 11th EUROMICRO Conference on Digital System Design Architectures, Methods and Tools, Parma, Italy, 2008, pp. 447-452, doi: 10.1109/DSD.2008.49.

[7] B. K. Bhoi, N. K. Misra, M. Pradhan, "A universal reversible gate architecture for designing n-bit comparator structure in quantum-dot cellular automata," *Int. J. Grid Distr. Comput.*, vol. 10, no. 9, pp.33-46, 2017.

[8] M D. Abdullah-Al-Shafi, A N. Bahar, "Optimized design and performance analysis of novel comparator and full adder in nanoscale," *Cogent Eng.*, vol. 3, 2016.

[9] Y.S. Xia, K.M. Qiu, Comparator design based on quantum-dot cellular automata, J. Electron Inform. Technol. 31 (2009) 1517–1520.

[10] Akter, Rubina & Islam, Nazrul & Waheed, Sajjad. (2015). Implementation of Reversible Logic Gate in Quantum Dot Cellular Automata. International Journal of Computer Applications. 109. 41-44. 10.5120/19155-0591.

[11] Anisur Rahman, Md & Sarker, Angona & Huq, Fazlul & Khatun, Fatema. (2013). Design and Implementation of Feynman Gate in Quantum-dot Cellular Automata (QCA). IJCSI International Journal of Computer Science Issues. 10. 167.

[12] S. Sinha Roy, C. Mukherjee, S. Panda, A. K. Muchopadhyay, B. Maji, "Layered T comparator design using quantum-dot cellular automata," *IEEE Conf. Dev. Integ. Circ. (DevIC)*, pp. 90-94, 2017.

[13] Sarker, MD. Badrul Alam Miah, "Design of 1-bit comparator using 2 dot 1 electron quantum-dot cellular automata," *Int. J. Adv. Comput. Sci. Appl.*, vol. 8, no. 3, pp. 481-485, 2017.

[14] M. Balali, A. Rezai, H. Balali, F. Rabiei, S. Emadid, "A novel design of 5-input majority gate in quantum-dot cellular automata technology," *IEEE Symp. Comput. Appl. Indust. Electr. (ISCAIE)*, pp. 13-16, 2017.

[15] Gao, M., Wang, J., Fang, S. *et al.* A New Nano Design for Implementation of a Digital Comparator Based on Quantum-Dot Cellular Automata. *Int J Theor Phys* (2020).

[16] Fengbin Deng, Guangjun Xie, Yongqiang Zhang, FeiPeng,Hongjun Lv, A novel design and analysis of comparator with XNOR gate for QCA,Microprocessors and Microsystems,Volume 55,2017,Pages 131-135,ISSN 0141-9331

[17] Hashemi, Sara & Navi, Keivan. (2014). Designing quantum-dot cellular automata circuits using a robust one-layer crossover scheme. The Journal of Engineering. 2014. 10.1049/joe.2013.0177.

[18] Sharma, VK. Optimal design for digital comparator using QCA nanotechnology with energy estimation. *Int J Numer Model*. 2021; 34: e2822.

[19] Thapliyal, Himanshu & Ranganathan, N. & Ferreira, Ryan. (2010). Design of a comparator tree based on reversible logic. 1113 - 1116. 10.1109/NANO.2010.5697872.

[20] Ramin Mokhtarii, Abdalhossein Rezai, J. Nano- Electron. Phys. 10 No 5, 05014 (2018)

[21] Waheed, Sajjad & Rasel, Md. (2017). Design and Implementation of New Feynman and Toffoli (NFT) Gates in Quantum-dot Cellular Automata (QCA). Circulation in Computer Science. 2. 64-67. 10.22632/ccs-2017-252-10.

 DOI : 10.35291/2454-9150.2021.0226