A New Fault Detection and Fault Tolerant Operation of Three Phase Interleaved DC-DC BoostConverters

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Abstract This paper presents a new method for fault detection in case of open circuit fault of switch and short circuit fault of inductor. One of the main attractions of this proposal is to provide a reliable operation of the converter, inorder to protect the converter from any external fault & to provide service continuity of loads connected to them. So that the quality of energy delivered by these converters can also be preserved. The proposed desaturation based fault detection for three phase interleaved boost converters uses voltage across the switch with respect to ground and control signals. A simple circuit with few general purpose devices are required for the fault detection. After detecting the fault in any of the converter power switches as well as inductors, the control of the converter is re-adapted to minimize the adverse impacts of faults, namely the increase of input current ripple. The new method can also reduce the fault detection time in converters. Inorder to prove the effectiveness of these strategies, the results are simulated using MATLAB.

Keywords —fault detection, open circuit fault, short circuit fault, current ripple, desaturation, interleaved boost converters

I. INTRODUCTION

The use of electronic equipment, as well as other DC-compatible loads witnessed a significant growth. Similar trend were followed by the distributed generation systems, that have spread in the last years. These two statements will trigger, the adoption of DC micro-grids in a near future, connecting distributed generation plants and consumers, with the reduction of the power conversion steps in mind. In a future where those grids will be used, several DC voltage levels will be required, enabling the connection of the several household DC loads. Using DC-DC converters in those grids will enable the use of such voltage levels.

In the current framework, ac–dc and dc–ac converters are fundamental in much of the office and domestic electric equipment. Unfortunately, the efficiency of these converters is quite limited, as the conversion process takes several steps to complete. A fault detection algorithm (FDA) and fault- tolerant control (FTC) scheme for switch OCF diagnosis in boost converter as proposed in [2] is very effective in terms of simplicity, short fault detection time and good voltage regulation. Several case studies pointed out the potential of dcmicrogrids and dc–dc converters to minimize the power losses at the residential energy distribution level [3]–[5]. Therefore, it is expected that low cost dc–dc power converters, able to ensure high efficiency, high reliability, and low output current ripple, will be frequently requested for such purposes.As power semiconductor devices are found to be the most fragile components. The faults in single or more components lead to degrade the system performance, discontinuity in the operation or damage of the whole system. Therefore, it is very essential to detect and isolate the faults for an efficient operation of the system. Even though fault diagnosis assumes a major importance, converter reconfiguration after a fault also plays an important role, otherwise it leads to an increase in in- put current ripple. In recent years, the thematic of diagnostic of open-circuit faults in the semiconductors of power converters have attracted the attention of many researchers. Several open-circuit fault diagnostic methods, applied to different dc–dc converter topologies, have been proposed in the literature.

To realize the fault diagnostic action, either time or frequency domain analyses are adopted to extract fault signatures from the diagnostic variables. The algorithms employing time- domain analyses are dominant. Commonly selected diagnostic variables include the transformer winding voltage [6], flying capacitor voltage [7], voltage of the magnetic components (inductors or transformers) [8], [9], derivative of the converter input current [10], inductor current [11], derivative of the converter inductor current [12]–[15], circulating current and/or submodules output voltage of the modular multilevel converter (MMC) [16], [17], converter input and output current, diode voltage or capacitors voltage. The algorithm based on the magnetic near field waveform falls into the group of algorithms based on frequency-

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domain analyses. Most of the aforementioned fault diagnostic algorithms are restricted to specific dc–dc converters; some focus certain operating points; while others have a broad spectrum of action, but are too complicated or have large fault diagnostic times. In [8], it aims to directly replace the faulty component or to support the converter operation during the postfault period. Albeit uncommon, the implementation of a redundant leg, aimed to directly replace a faulty converter leg is also feasible. In fewer converter topologies, the intrinsic converter semiconductors assured the bypass functions [10].

Phase-shift adjustment is a suitable reconfiguration strat- egy for converter topologies which apply phase-shift control strategies, as it is the case of the interleaved dc–dc converter [12], or the parallel-connected single active bridge dc–dc converter [13]. Unfortunately, phase-shift adjustment is unable to banish all side-effects of open-circuit faults. To override the pitfalls, improved diagnostic capabilities and broadened spectrum of action of the fault diagnostic principles used in [10], is reshaped. The oscillations of the converter input current are subjected to a normalization procedure. After detecting a fault, the converter operation is reconfigured: phase and frequency of each pulsewidth modulation (PWM) gating signals are adapted according to the detected fault mode. More recently, the emergence of sophisticated DSPs triggered the development of fault diagnostic algorithms based on the model of the dc–dc converter. The derivation of such converter models may be particularly challenging in converters with a significant number of components. Moreover the real- time emulation of the converter response implies a significant computational effort. Even though fault diagnosis assumes a major importance, converter reconfiguration after a fault also plays an important role. In dc–dc converter topologies based on a modular architecture, additional discrete components are arranged in such a configuration that allows to bypass the faulty module.

This paper proposes a fault detection method featuring low complexity, low cost, high reliability, and efficiency within a single solution. After detecting a fault, the converter operation is reconfigured: phase and frequency of each pulsewidth modulation (PWM) gating signals are adapted according to the detected fault mode.

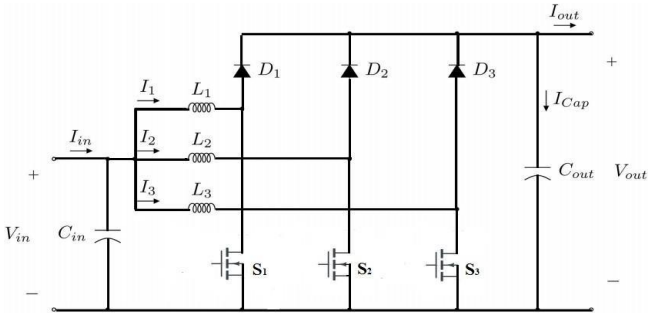

Fig. 1. Block diagram of proposed fault detection and fault tolerant operation of converter

II. CONVERTER OPERATION

Interleaved boost converter is used in high power applica tion. The challenge of designing boost converter is to handle high current and voltage at input and output.The input current and output voltage ripple of interleaved boost dc-dc converter can be minimized by virtue of interleaving operation. Input current can be shared among the other phases. The three phase interleaved boost dc-dc converter consists of three parallel connected boost converter units, which are controlled by a phase-shifted switching function (interleaved operation). This converter has three parallel units. A phase shift should be implemented between the timing signals of three switches. There are voltage multiplier units between the phases for increasing the output voltage.

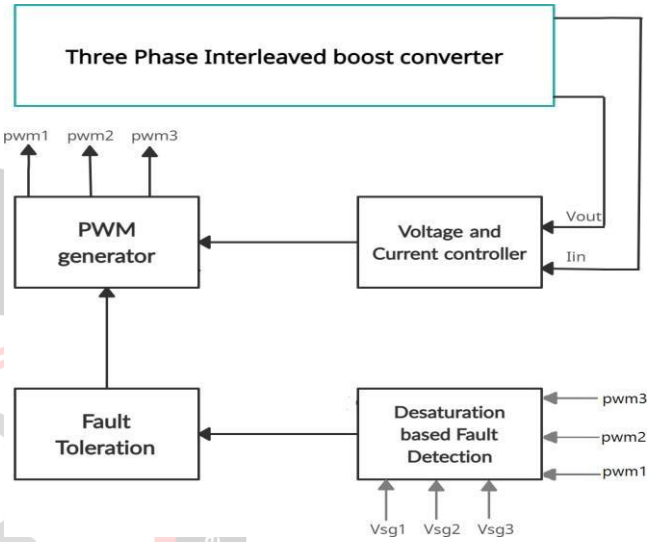

Fig. 2. Three phase interleaved boost converter

Fig.2 depicts the three-phase non-isolated interleaved boost converter. The interleaved boost converter with three phases provides a good balance between simplicity and efficient power management.

The converter input current comprises the sum of each phase current

$$I_{in} = I_1 + I_2 + I_3$$

Based on above equation, the derivative of the converter input current dI_{in}/dt comprises the sum of the derivatives of each phase

$$\frac{dIin}{dt} = \frac{dI1}{dt} + \frac{dI2}{dt} + \frac{dI3}{dt}$$

Taking into account the identical nature between phases, an analysis will be performed for just one converter phase. When the power switch S1 is conducting, the derivative of e inductor current dI_1/dt will be given by,

$$\frac{dI1}{dt} = \frac{Vin}{L1}$$

Meanwhile, when the switch is OFF, the derivative of the current flowing through the inductor dI_1/dt is given by

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$$\frac{dI1}{dt} = \frac{Vin - Vout}{L1}$$

Considering the ideal model of the interleaved boost converter, the voltage gain of the interleaved boost converter is expressed as follows:

$$\frac{Vout}{Vin} = \frac{\mathrm{DM}}{DM - D}$$

where D_M denotes the period of non-zero inductor current and D denotes the switching duty cycle.

After an open-circuit fault in a switch, no current flows through it. Thus, only (4) will be verified; the phase current will decrease linearly, reaching zero phase-current soon. It can be concluded that I_{in} derivative becomes positive under healthyoperation and I_{in} derivative becomes negative after an open circuit fault operation

$$\frac{dI1}{dt} = \begin{cases} \frac{Vin}{L1}, & for\ 0 \le t \le DT \\ \frac{-Vin * D}{L1(DM - D)}, & for\ DT \le t \le T \end{cases}$$

III. FAULT DETECTION

The proposed fault detection method is achieved using very few components. The Voltage across the switch is used for fault diagnostic purposes inorder to achieve fast fault detection. Using V_{sw} with respect to the ground and the control signals together, OCF across each switch and SCF through inductors can be detected.

During the normal operation of converter, when PWM pulse is at positive peak, the switches becomes ON and experiences an approximately zero voltage across it. So the ON period of each switch does not charge the capacitor and output voltage is zero. When one switch turns OFF during the zero voltageof the PWM, capacitor output voltage is zero for normal operation of the converter. The occurrence of OCF in any switch causes voltage across that switch to rise immediately to high level. Now, the capacitor voltage changes from zero voltage to switch voltage level. If fault tolerant operation is not employed, the output capacitor voltage builds up for next few PWM cycles. The capacitor voltage is compared with the threshold voltage to generate final FD pulse. The time at which the FD pulse is generated depends on the rate of rise of the output capacitor voltage which is a function of PWM frequency, RC value and switch voltage. Also, after the fault detection, the converter has a tendency in increasing the input current ripples which can be lowered by the fault tolerantoperation.

A. Desaturation based fault detection for low Voltage Power MOSFET

During the on-state of the power MOSFET a small addi- tional current is injected into the power stage. So that the actual drainsource voltage of the low voltage power MOSFET V_{DS} and the forward voltage drop V_F of the Diode D_1 is measured and divided by a voltage divider as shown in fig.

Then this voltage over R_3 is compared with a reference voltage V_{ref} by a fast comparator. If the measured voltage V_{DS} +V_F is higher than the reference voltage, which means that a failure has occurred or the MOSFET is blocking, the output voltage V_1 of the comparator is set to the high level.To decrease the temperature dependence of the desaturation detection circuit the reference voltage V_{ref} depends on themeasured case temperature T_C of the power device, which is nearly the junction temperature T_J in steady-state, by a thermistor. With increasing temperature the resistance of the thermistor decreases and leads to a higher reference voltage V_{ref} . After the detection of a too high drain-source voltage, which is also present during the blocking time of the power MOSFET, the fault signal of the comparator is filtered with a time constant of a few picoseconds. The following RS flip-flop has the function to hold the failure signal and to disable the detection circuit during the blocking time by means of IN=0.The flip-flop is being reset by the next high level of the logic input signal IN. Using a RS flip-flop as an integrated circuit instead of a discrete solution leads to a lower circuit volume, a low propagation delay and low costs.

The input signal IN is just applied to the driving stage, whenthere is no detected failure, which is done by an AND-gate. Otherwise the input signal of the driving stage is hold down at the low level. Finally the control signal is applied to the MOSFET driver.

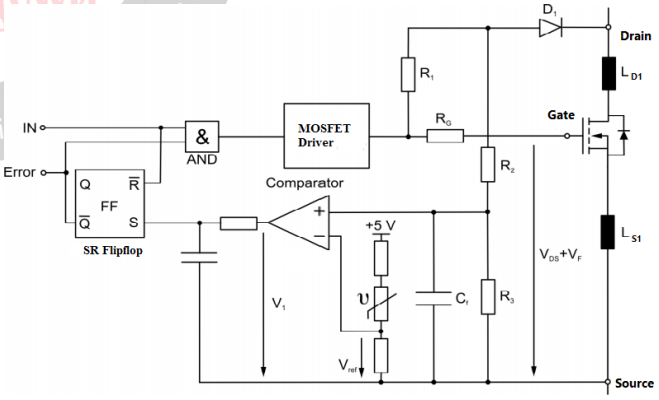

Fig. 3. Desaturation detection circuit for low voltage power MOSFETs

IV. FAULT TOLERANT OPERATION

A control strategy consisting of 8 combinations of adap- tive phase shift and frequency variation can perform the reconfiguration after a fault with good results. The operationof interleaved dc–dc boost converters under fault conditions has critical side-effects, especially when no re-configuration measures are developed

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1) Increment of the converter input current ripple.
2) Poor current sharing among the healthy converter phases.
3) Additional current ripple in the converter output electrolytic capacitor, leading to overheating and consequent curtailment on the capacitor useful lifetime

Phase-shift correction is typically adopted in the reconfig-uration of faulty interleaved dc–dc converters. This action reduces, in general, the converter input current ripple after a fault. Unfortunately, it does not allow to re-establish prefault ripple levels. Therefore, additional actions can be taken to reduce the ripple even more.

A. Phase-Shift Correction

According to the information available in the controller regarding the presence and location of fault, this component provides information about the phase shift to apply between each PWM signal. In general, this component defines a phase shift of π rad between PWM signals assigned to the healthy converter switches.

B. Switching Frequency Correction

The switching frequency f_{sw} assumes predefined discrete values. The increment of f_{sw} during the postfault period aims to re-establish the frequency of the current ripple to prefault levels. A pretty good estimation of the switching losses P_{sw} occurring in one converter switch can be obtained using the following relation,

$$Psw = (Eon + Eoff) * \frac{VDC}{VDC, norm} * \frac{IC, pk}{Ic, norm} fsw$$

where Eon denotes the energy dissipated during the turn-ON period, E_{off} refers to the energy dissipated during theturn OFF period, V_{DC} denotes the measured converter input voltage, $V_{DC,nom}$ refers to the switch rated dc-link voltage, I_C,pk denotes the measured peak switch current, I_C,nom denotes the nominal switch current, and f_{sw} denotes the switching frequency. E_{on}, E_{off}, $V_{DC,nom}$, and $I_{C,nom}$ are constants that are definedin the datasheet of the switch. On the other hand, the peak switch current $I_{C,pk}$ and the switching frequency f_{sw}, both measured during the postfault period, increase by 1.5 times in comparison to the prefault values

$$I'c, pk = 1.5 * Ic, pk$$
$$fs'w = 1.5 * fsw$$

Therefore, the relation between the switching losses at the post- fault period P'_{sw} and prefault period P_{sw} is

$$P'sw = \frac{9}{4} * Psw$$

The implementation of this reconfiguration strategy contributes to a part of the increment on the overall switching losses. Additional switching losses occur during the postfault operation of the converter, regardless of the implementation of reconfiguration measures. As f_{sw} increases by 1.5 times during the postfault period, when compared to the f_{sw} during the pre- fault period, the increment of f_{sw} solely contributes by 1.5 times to the overall increment of the switching losses verified in the postfault period.

V. SIMULATION RESULTS AND DISCUSSION

To confirm the effectiveness, a simulation model of the proposed fault detection & fault tolerant operation of three phase interleaved boost converter is implemented in MAT-LAB/ Simulink environment. The OCF in any of the switches & SCF through inductors in three phase interleaved boost converters can be detected using the desaturation based fault detection and the fault can be tolerated or the converter can reconfigured using the fault tolerant operation.

A. Simulation Parameters

The main parameters used in this simulation are summarized in Table 6.1. The values of the passive elements used are 7.6mH for inductance L_1, L_2, L_3 and 680μF for output capacitance. The input voltage of 24V is applied for a load resistance of 30Ω. The converter is switched at 20kHz.

TABLE I SIMULATION PARAMETERS

Parameter	Symbol	Value/Number
Input Voltage	Vin	24
Inductance	Li	7.6mH
Input capacitance	Cin	$72\mu F$
Output capacitance	$Cout$	$680\mu F$
Load resistance	Ro	30Ω
Switching frequency	fsw	20Khz

B. Simulation Results

1) *Converter Operation*: The results are obtained for Con-verter operation, fault detection and fault tolerant operation. For an input voltage of 24V, output is obtained as 48V. Also the switching pulses and inductor currents charging and discharging for each phases are obtained for a duty cycle of 50% as shown below.

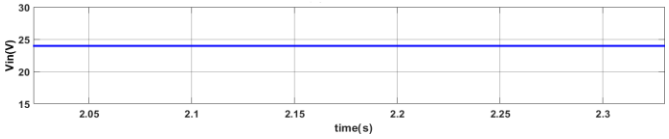

Fig. 4. Input voltage of converter, V_{in} = 24V

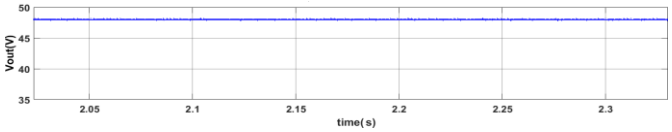

Fig. 5. Output voltage of converter, V_{out} = 48V

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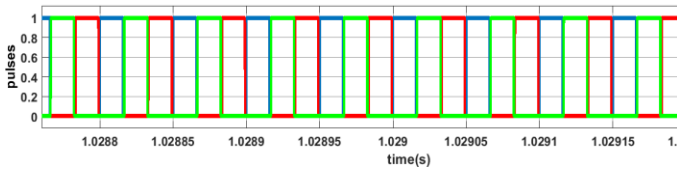

Fig. 6. Switching pulses with D=50%

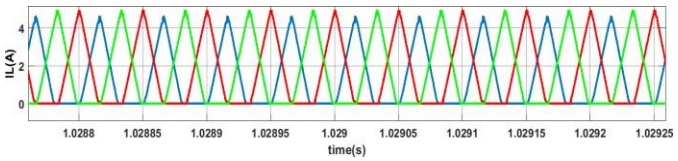

Fig. 7. Input phase currents through inductors

C. *Fault Detection*

Fault detection is performed by comparing the voltage across the switches and control signals, at each sampling time. A fault is determined to have occurred whenever the output is high and when the output is low, converter is said to be under healthy condition. An OCF is detected across the switch at 1 sec as shown below. Here the faultoccurence and fault detection are closer to each other, hencethe fault detection time is of μs range

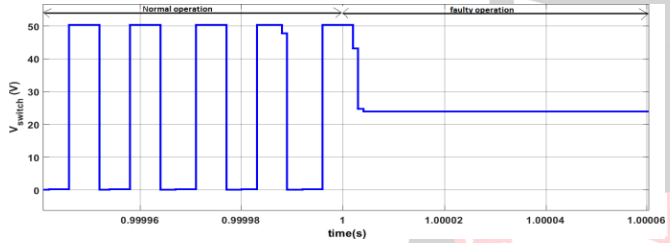

Fig. 8. Voltage across the switch under fault at S_1

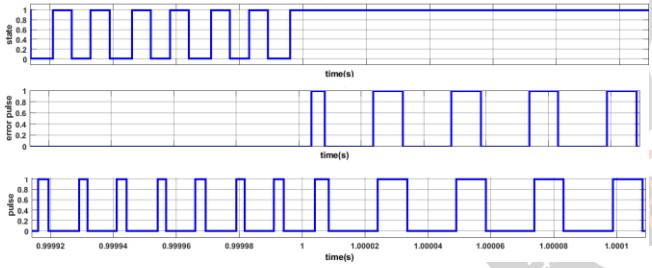

Fig. 9. waveforms of relational operator output, errorpulse and PWM pulsefor a fault at 1 sec.

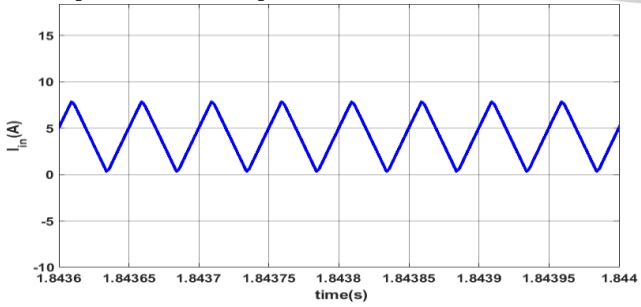

Fig. 10. Input current without any reconfiguration

Fig. 8 & 9 show the experimental results of the fault detection method under the OCF in switch S_1 or SCF in L_1. It can be seen from Fig. 8 that the fault has occured at 1 sec and is being detected after μs range. When the fault occurred, the switch S_1 was in ON-state, and since the fault causesthe immediate increase of the inductor current, the error is immediately observed. The OCF fault is occurred at 1 sec,and through applying the proposed fault detection method, thefault is detected immediately.

During faulty condition, the input current has a tendency in increasing the ripples higher than that in the healthy condition. After a fault, the ripple of I_{in} increases almost twice. Here we can see the input current ripple as 7.54A which is very much higher than the healthy condition input current ripple (0.984).

D. *Converter Reconfiguration after Fault*

In the phase shift correction simulation environment, each signal introduced in this component is delayed by one sampling period to avoid algebraic loop errors. According to the information given to this block about the presence and locationof faulty phases, the outputs will change the values sent to the PWM generator.

As MOSFET S_1 is under faulty condition after 1 sec, the other two phases are provided with a phase shiftof 180deg and switching frequency is increased to 1.5 times the prefault f_{sw} as shown in fig. 11.

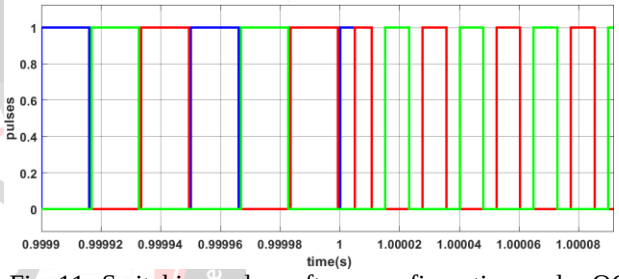

Fig. 11. Switching pulses after reconfiguration under OCF in S_1

When a fault has occured in S_1 & S_2, after 1 sec, the third phase is only under operation with a switching frequency increased 3 times the prefault f_{sw} as shown in fig. 12.

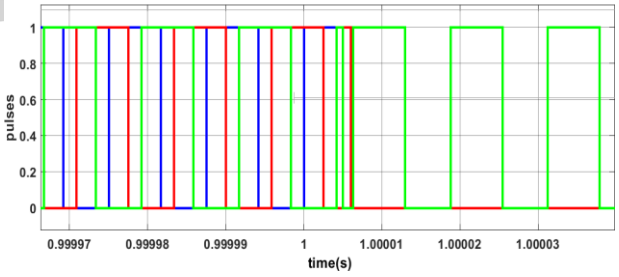

Fig. 12. Switching pulses after reconfiguration under OCF in S_1 & S_2.

When a SCF has occured in L_2, then the corresponding S_2 can behave as an OCF. Hence phase 1 and 2 are under operation with 180 deg phase shift between them and f_{sw} is increased to 1.5 times the prefault value as shown in fig.

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13.

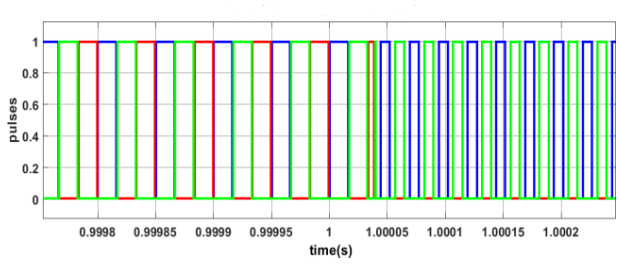

Fig. 13. Switching pulses after reconfiguration under SCF in L_2.

Despite the fact that phase shift plays an important rolein ripple minimization after an open-circuit fault, further improvements in the limitation of ripple are also attained after combining the increase of f_{sw} with phase-shift correction. As the tendency in increasing the input current ripple is suppressed using the reconfiguration strategy (phase shift correction & switching frequency correction) with input current ripple being 0.942A. It can be seen in fig. 14 that ripple is reduced below the healthy condition ripple value with output power of 100W.

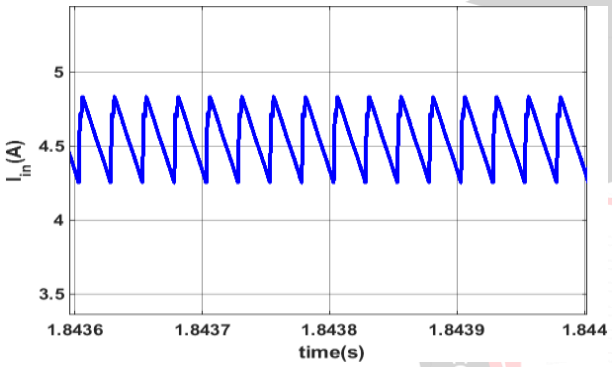

Fig. 14. Input current after full reconfiguration

The output voltage waveform after reconfiguration canbe seen from fig. 15 ie, obtained by the fault tolerant operation(Phase shift correction & switching frequency correction) in the most prominent and feasible method available.

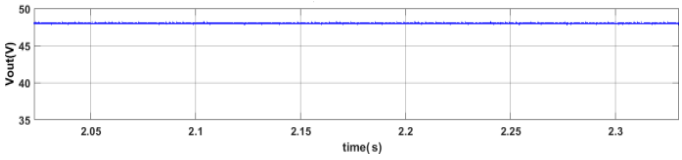

Fig. 15. Output Voltage after reconfiguration

Experimental data shows the effectiveness of the reconfiguration strategy used. A significant increment in the ripple of I_{in} is observed, as one of the converter phases stopped working. At the same time, the remaining phases are controlledresorting to an unbalanced switching pattern. When reconfig- uration strategy is applied, the switching pattern balance is re-established and the switching frequency fsw increases from 1 to 1.5 kHz. Ripple levels are further reduced.

TABLE II RECONFIGURATION PERFORMANCE METRICS

In order to show the benefits of reconfiguration strategy, Table II establishes a comparison between the different reconfiguration scenarios. Data was collected from the experimentalresults and compiled in the form of distinctive

f_{sw}	P_{out}	Metrics	Healthy	Faulty, no reconfiguration	Faulty, full reconfiguration
20kHZ	100 W	ΔI_{in}[A]	0.984	7.54	0.942
		ΔI_{cap}[A]	0.007	0.024	0.008
		η [%]	95.04	88.72	94.89

performance metrics: relative input current ripple (ΔI_{in}), output capacitor current ripple (ΔI_{Cap}), and converter efficiency (η).

These performance metrics are mathematically defined usingthe following expressions:

$$\Delta I_{in} = I_{inmax} - I_{inmin}$$

$$\Delta I_{cap} = I_{capmax} - I_{capmin}$$

$$\eta = \frac{\text{Pout}}{\text{Pin}} * 100$$

The above mentioned performance metrics are based on data obtained along the postfault converter operation, when steady-state conditions are recovered. Based on the results available at Table II, it is stated that the adoption of reconfiguration strategy successfully accomplishes the objectives of reduction of the side-effects of faults, with minimal negative impact on the loss of power conversion efficiency.

E. Comparison of the Results with other Methods

Table III gives the information needed to evaluate the performance of fault diagnostic methods, suitable for the diagnostic of switch failures, available in some of the literature. Inorder to prove the effectiveness of diagnostic methods available, researchers focused more totechnologies with different degrees of complexity, computational power, and cost. For that reason, the evaluation of the diagnostic action quickness versus the implementation complexity reveals as critical.

TABLE III COMPARISON WITH OTHER FAULT DIAGNOSTIC METHODS

Diagnostic Variable	**Converter topologies**	f_{sw}	t_d *max*
Input current derivative sign	Interleaved boost converter	1 kHz	2 T_{sw} (2ms)
Inductor current emulation	Non-isolated DC-DC converters	10 kHz	T_{sw} ($100\mu s$)
State estimation	Switching power converters	10 to 20 kHz	10 ms
Inductor current derivative sign	Non-isolated single-switch converters	15 kHz	T_{sw} ($67\mu s$)
Mosfet Voltage	Interleaved boost converter	20 kHz	T_{sw} (25)

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f_{sw} – switching frequency

t_{d_max} - maximum fault detection time

T_{sw} – switching period

As stated in Table III, the proposed fault detection strategy provides remarkable capabilities to detect faults in a short period of time, with a small computational effort. When compared to other fault diagnostic strategies, the proposed strategy reaches the minimum fault detection time. Such performance lies on the fact that the proposed fault diagnostic method in interleaved converters resorts to simple manipulation of the converter variables and their values, without requiring complex mathematical computations or emulation of the converter model.

VI. CONCLUSION

The use of DC-DC converters is gaining importance. Until now, DC-DC converters were mainly dedicated to industrial applications. However, these converters may become part of our home appliances soon, as concerns about our dwelling's energy efficiency increases. Many of our home appliances require power converters with high reliability levels, in order to extend the lifespan of those appliances.

These converters, like any other converter, may suffer faults that degrade their smooth operation, compromising the converters themselves as well as the load connected to them, reducing their lifespan. Desaturation based fault detection method is carried out using a simple circuit which comprises general purpose devices.The converter behavior forboth normal and faulty operations have been identified. The simulation results show the effectiveness of the fault detection proposed and fault tolerant control strategy. Reliability and satisfactory converter performances are achieved. The input current and output voltage ripples significantly decreased, providing the similar converter performances compared with healthy operation. This system has presented fault detection and fault reconfiguration strategies applied to OCF in the power switches & SCF through inductors of a multi-phase DC-DC converter with reduced fault detection time. Regardlessof that, these strategies can be used for many other DC-DC converter topologies.

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