A Comprehensive Review of Multi-Level Inverters for High-Power Microgrid Applications

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Abstract - This paper presents a comprehensive review of multilevel inverters (MLIs) for high-power microgrid applications. MLIs have emerged as a pivotal technology for efficiently converting DC to AC power in renewable energy systems and high-power applications. This review covers various multilevel inverter topologies, including diode-clamped, flying capacitor, and cascaded H-bridge configurations, highlighting their operational principles, advantages, and limitations. The cascaded H-bridge inverter is noted for its minimal component requirement and high stepped output, making it a preferred choice for scalable and flexible microgrid systems. The paper also discusses innovative topologies and advanced pulse width modulation (PWM) techniques aimed at reducing total harmonic distortion (THD) and improving overall inverter performance. Simulation results comparing different PWM methods indicate that multicarrier PWM techniques are more effective in minimizing THD compared to conventional approaches. Additionally, the impact of amplitude modulation index on harmonic performance and filter design is analyzed. This review provides valuable insights into the selection and implementation of MLIs in high-power microgrids, emphasizing the importance of optimizing inverter design for enhanced efficiency, reliability, and scalability.

Keywords - Microgrids, Renewable Energy Sources, Multi-level Inverters, Renewable Energy, Inverter Topologies.

I. INTRODUCTION

The term "Multi-Level Inverter" (MLI) refers to a specific kind of power electronic system that converts several levels of direct current (DC) into alternating current (AC). When compared to traditional two-level inverters, this technology provides a number of benefits that make it especially appealing for applications that need medium to high voltage. Multilevel inverters are used in power conversion systems because of the enhanced waveforms that they produce for both voltage and current. Because of their benefits over traditional inverters and their capacity to eliminate undesired harmonics, they have lately emerged as key alternatives in high-power medium voltage applications. This is due to the fact that they are able to improve system performance and efficiency (Pharne and Bhosale, 2013). To achieve greater power quality and higher voltage capabilities, the idea of multilayer inverters attempts to eliminate switching losses and get output voltage with many stages. This is done in order to accomplish the desired results. High voltage AC motor drives, distributive generation, high voltage direct transmission, and SVC applications are all examples of applications that make use of multilevel inverters (Prasad et al, 2013). There have been a number of studies that have investigated the various topologies and features of multilayer inverters. A comprehensive analysis of the topology of multilevel inverters has been carried out. CMLI has been addressed from a variety of topological perspectives (Lakshmi et al, 2013). Our investigation focused on a cascaded seven-level inverter that used the level shifting pulse width modulation (PWM) approach and had a decreased number of switches. There has been an analysis performed on a novel topology for a multilayer inverter design (Najafi et al, 2012). There has been a new multilevel converter architecture implemented, which decreases the amount of switches that are required. The problem of a five-level inverter architecture that uses a single DC source and is solved by cascading a flying capacitor inverter has been encountered (Roshankumar et al, 2012). A multilayer inverter that has a lower number of switches has been proposed as a solution. An evaluation has been conducted on a brand new 81-level inverter that has a decreased number of switches. There is a novel cascaded multilevel inverter that has been suggested, and it involves fewer switches than its predecessor. It has been suggested that a multilayer inverter with a lower number of switches become available. There has been discussion of a multi-level inverter that is able to regulate the power factor (Jacob et al, 2012).

It has been reported how a diode-clamped multilevel inverter may operate in a quasi-two-level and three-level configuration by using space vector modulation. In order to get the greatest possible number of levels from the DC sources that are available, an architecture for multilevel inverters has been developed (Rahilal et al, 2012). It has been determined that symmetrical and asymmetrical multilevel inverters are identical in their operation. It has been proposed that high voltage applications might benefit from a novel architecture of cascaded multilevel converters that has a decreased number of components (Babaei, 2012). A discussion has taken place on the idea of a symmetrical hybrid multilevel inverter that is based on multistate switching cells. There has been a description of a voltage-

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source inverter that has several levels and two levels of power modules (James et al, 2012). There has been a suggestion made for a transistor-clamped H-bridge that incorporates a novel approach to capacitor voltage balancing. There has been a suggestion made for a novel multilevel inverter architecture that makes use of a reduced number of switches (Sun et al, 2012). It has been proposed that an asymmetrical multilevel inverter for traction drives that only requires one DC supply may be used. Several other multilayer inverter topologies, each with a decreased number of switches, have been investigated (Adam et al, 2012). There is a new multilevel inverter architecture that has been developed, and it features a decreased number of switches. It has been suggested that a modified cascaded multilevel inverter that makes use of bypass diodes and has a lower switch count might be beneficial. The development of a class of cascaded multilevel inverters that are capable of regeneration and have a decreased number of switches has taken place (Gupta et al, 2012). It has been detailed how multilevel inverter topologies may be used for stand-alone photovoltaic systems. There has been an investigation of a unique multilayer inverter. A comparison of multilevel inverters that are considered to be state-of-the-art has been done. An investigation has been conducted on a unique multilevel inverter architecture that does not include any clamping diodes or flying capacitors (Lakshmi and Chandra, 2012). The development of a revolutionary modulation method for multilevel inverters may be attributed to the use of comparable area. Through the use of simulation, research has been carried out on a variety of multilevel inverter control strategies (Ebrahimi et al, 2011). There has been discussion of a cascade multilayer inverter that makes use of a single DC source. There is a novel topology for a multilayer inverter that has been presented (Caballero et al, 2011). The description of a unique hybrid multilevel inverter that makes use of DC-link voltage combination has been submitted. An investigation on the topologies, controls, and applications connected to multilevel inverters has been carried out (Suroso et al, 2011). In order to facilitate the deployment of FACTS controllers, it has been suggested to provide a comparison of high power converter topologies (Rahim et al, 2011). A generalised under-land snubber that is designed for use with flying capacitor multilevel inverters and converters has been put into development. The introduction of a control topology for single-phase UPS inverters brought about this development (Murugesan et al, 2011).

II. Various Multilevel Inverter Types

Multilevel inverters are becoming more common in the electricity market in today's world. It begins with an inverter that has three levels. When it comes to the operation of multilevel inverters, one of the most significant problems is the unbalanced voltage (Dixon et al, 2010). The following categories are used to categorise the multilayer inverters:

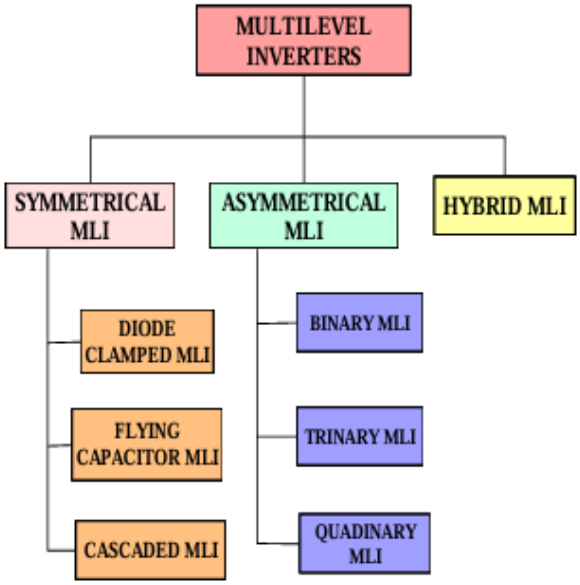

Fig 1: Various Multilevel Inverter Types

III. Topologies for Multilevel Inverters

There are three primary types of multilevel inverter topologies: symmetrical, which has source voltages that are equal to one another, asymmetrical, which has source voltages that are not equal to one another, and hybrid inverters (Rokan et al, 2010).

3.1 Multilevel Inverters with Symmetry

What is meant by the term "symmetrical multilevel inverter" is an inverter that has voltage sources that have the same amplitude (Arif et al, 2009). Take, for instance, the case when one source is supplied with 100V of DC sources; this means that all sources have 100V.

3.1.1 Multilevel inverter with diode clamping

The primary idea behind this inverter is to make use of diodes in order to reduce the voltage stress that is placed on power equipment. Each capacitor and switch has a voltage of V_{dc} that is measured over them. (m-1) voltage sources, (m-1) capacitors, 2(m-1) switching devices, and (m-1) (m-2) diodes are required for each leg of an inverter that operates at the m level.

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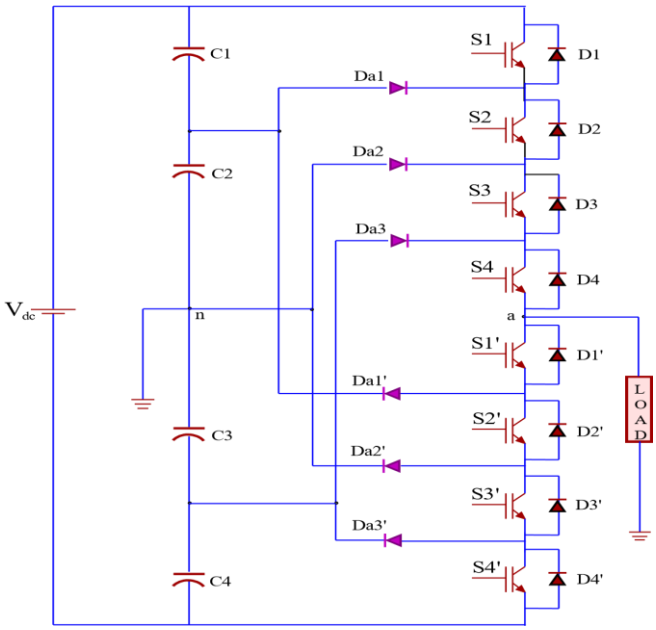

Fig 2: Multilevel inverter with five levels of diode clamping

Table 1: Switch states and levels of output voltage in a diode-clamped inverter

Switch state								Output
S1	S2	S3	S4	S1'	S2'	S3'	S4'	V_{an}
1	1	1	1	0	0	0	0	$+V_{dc}/2$
0	1	1	1	1	0	0	0	$+V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

3.1.1.1 Operating Principle

Let us take into consideration simply one leg of the five-level inverter, as seen in figure 2, as an example, in order to generate a voltage that is comparable to that of a staircase. The illustration in figure 3 depicts a bridge that is single-phase and has two legs. As the reference point for the output phase voltage, the dc rail 0 is the point of reference. These are the steps that need to be taken in order to synthesise the five level voltages:

1. To get an output voltage level of $va0 = V_{dc}$, activate all of the switches in the top half, Sa1 through Sa4.
2. Turn on two upper switches, S_{a3} through S_{a4}, as well as two lower switches, S'_{a1} and S'_{a2}, in order to achieve an output voltage level of $_{va0}$ equal to $V_{dc}/2$ or higher.
3. Ensure that all lower half switches, S'_{a1} through S'_{a4}, are activated in order to achieve an output voltage level of $v_{a0} = 0$.

The switch is switched on when it is in state condition 1, and it is turned off when it is in state condition 0. It is important to take note that each switch is activated just once throughout each cycle, and that there are four switch pairs that are complementary to one another in each phase. The pairings that correspond to one leg of the inverter are respectively denoted as (S_{a1}, S'_{a1}), (S_{a2}, S'_{a2}), (S_{a3}, S'_{a3}), and (S_{a4}, S'_{a4}). As a result, if one of the switch pairs that are complimentary is activated, the other switch pair in the same pair must be deactivated. It is always the case that four switches are activated at the same time. It is the positive phase-leg voltage of terminal a that makes up the line voltage, and the negative phase-leg voltage of terminal b that makes up the line voltage. One half of the sinusoidal wave is tracked by each phase-leg voltage throughout the process. The line voltage that is produced is a staircase wave with five levels respectively. In light of this, it may be deduced that a converter operating at the m level has a phase-leg voltage at the *m* level and a line voltage at the (2*m-1*) level.

It is important to calculate the switching angles in such a manner that the total harmonic distortion (THD) of the output voltage is reduced to the lowest feasible value. The harmonic elimination approach is the method that is used in this thesis for the purpose of calculating the switching angle. Utilising this technique, it is possible to get rid of the lower dominant harmonics by selecting switching angles that have been computed.

3.1.1.2 Features

1. Blocking diodes need a high voltage rating in order to function properly.
2. Device ratings that are not equal.
3. The voltage of the capacitor is irregular.

3.1.1.3 Advantages

1. Superior effectiveness.
2. In order to decrease harmonics, filters are not required.
3. Control is possible over the flow of reactive power.
4. Uncomplicated is the control approach.

3.1.1.4 Disadvantages

1. Additionally, a greater quantity of diodes is necessary at high levels.
2. The actual regulation of the flow of electricity for each individual converter is challenging.

3.1.2 Multilevel Inverter with Flying Capacitors

Capacitors are an essential component of this inverter because they limit the voltage that is delivered to the power devices, which guarantees that the device will function in a secure and effective manner. These capacitors are used to divide the input DC voltage, which is crucial for the performance of the inverter. In addition to their main role of restricting voltage, these capacitors were also utilised to limit voltage. The general construction of the flying capacitor multilevel inverter is very similar to that of the diode clamped multilevel inverter, despite the fact that this main difference exists between the two technologies.

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There is a voltage value of Vdc that is consistent across all of the components of the system, and this voltage value is used to characterise each capacitor and switch. During the whole of the inverter's operation, this consistency is essential for preserving both stability and performance. The flying capacitor-based multilevel inverter's design is shown in Figure 3, which gives a visual depiction of the architecture and illustrates the intricate interconnections and operation, respectively.

It is essential for the dc bus form level converter to include a certain quantity of capacitors, namely (*m-1*) capacitors, in order for the inverter to function in an efficient manner. By adhering to this condition, the inverter is guaranteed to be able to effectively regulate voltage levels, produce the required output, and keep its operational integrity intact. A vital component of the inverter's performance and dependability in a variety of applications is the careful arrangement and integration of these components.

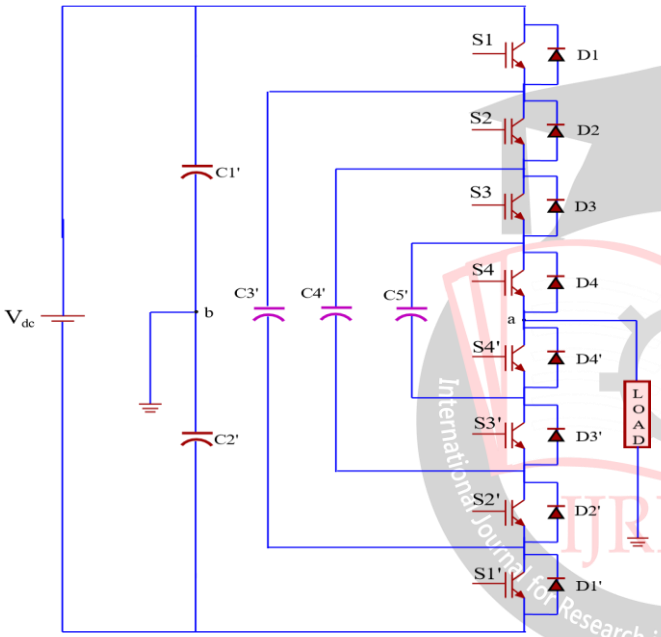

Fig 3: Five-level flying capacitor multilevel inverter.

Table 2: This multilayer inverter is built on a five-level flying capacitor basis.

S1	S2	S3	S4	C3'	C4'	C5'	V_{ab}
0	0	0	0	NC	NC	NC	$-V_{dc}/2$
0	0	0	1	NC	NC	-	$-V_{dc}/4$
0	0	1	0	NC	-	+	
0	1	0	0	-	+	NC	
1	0	0	0	+	NC	NC	
1	1	0	0	NC	+	NC	0
1	0	1	0	+	-	+	
1	0	0	1	+	NC	-	
0	1	1	0	-	NC	+	
0	1	0	1	-	+	-	
0	0	1	1	NC	-	NC	
0	1	1	1	-	NC	NC	$-V_{dc}/4$
1	0	1	1	+	-	NC	
1	1	0	1	NC	+	-	
1	1	1	0	NC	NC	+	
1	1	1	1	NC	NC	NC	$-V_{dc}/2$

3.1.2.1 Features

1. Large quantity of capacitors in use.
2. Adjusting the voltages of the capacitors.

3.1.2.2 Advantages

1. During a power outage, additional ride through capability is available.
2. In order to decrease harmonics, filters are not required.
3. The appropriate switching combination is provided, allowing for the balancing of various voltage levels.
4. One is able to exert control over both real and reactive power flow.

3.1.2.3 Disadvantages

1. When it comes to high level, a significant number of capacitors are necessary.
2. Real power transmissions have a high switching frequency, which results in significant losses.

3.1.3 Cascade multilevel inverter

"The purpose of this inverter is to generate a sinusoidal voltage output by linking H-bridge inverters in series. This is the notion that underpins this instrument. When the voltage that is produced by each individual cell is joined with the voltage that is produced by the system as a whole, this arrangement serves as the basis for the system. The total number of output voltage levels is twice the number of cells plus one, which enables more flexibility in output. This is an important point to observe.

The ability to utilise switching perspectives in a strategic manner is one of the most significant benefits of this method. A cleaner and more efficient output may be achieved by optimising these angles, which will result in a considerable reduction in the total harmonic distortion. In applications that need a power supply of high quality, this is an absolutely necessary component.

Moreover, in comparison to conventional arrangements, such as diode clamped or flying capacitor inverters, this particular form of multilayer inverter has a number of advantages. One of the most notable benefits is that it needs less components, which helps to reduce the total weight of the inverter as well as the expenses associated with its production. Not only does this make the inverter more economical, but it also makes it simpler to install and incorporate into a variety of different sets of requirements. An excellent solution for attaining efficient power conversion while preserving a small and cost-effective form factor is provided by this revolutionary design, which is the outcome of the aforementioned impact.

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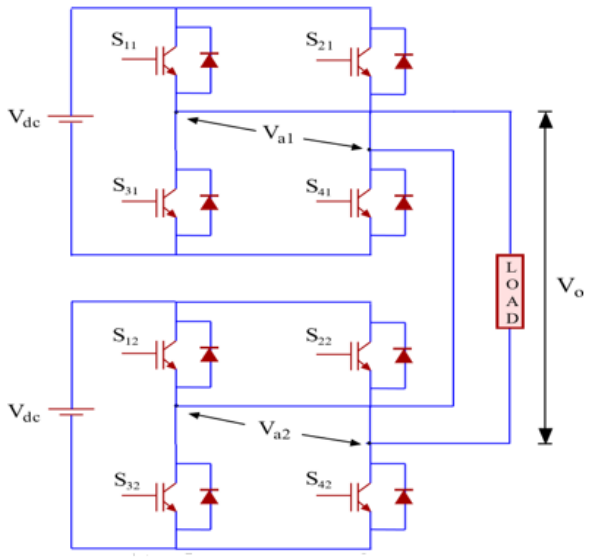

Fig 4: Multilevel inverter with five cascaded levels

The illustration in Figure 4 is an example of a cascaded H-bridge multilevel inverter with five levels. Using a manner that is compatible with the approaches employed in prior multilevel inverter designs, this inverter uses a way for computing switching angles. This ensures compatibility and makes it easier to implement. Two switching devices are required for each output voltage level of a cascaded H-bridge multilevel inverter with m levels. The term "m" refers to the total number of voltage levels that are generated. This is necessary for the inverter to function correctly. Therefore, the general architecture of the inverter is simplified as a result of this design, which eliminates the need for extra clamping diodes or capacitors that would otherwise be necessary to adjust the voltage. As a consequence of this, the cascaded H-bridge multilevel inverter is capable of achieving effective voltage control while keeping a compact construction. As a result, it is a plausible option for a variety of applications concerning power electronics.

Table 3: Switch states and voltage levels of five level cascaded inverter

S_{11}	S_{21}	S_{12}	S_{22}	Output (V_o)
0	0	0	0	0
0	0	0	1	$-V_{dc}$
0	0	1	0	$+V_{dc}$
0	0	1	1	0
0	1	0	0	$-V_{dc}$
0	1	0	1	$-2V_{dc}$
0	1	1	0	0
0	1	1	1	$-V_{dc}$
1	0	0	0	$+V_{dc}$
1	0	0	1	0
1	0	1	0	$+2V_{dc}$
1	0	1	1	$+V_{dc}$
1	1	0	0	0
1	1	0	1	$-V_{dc}$
1	1	1	0	$+V_{dc}$
1	1	1	1	0

3.1.3.1 Features

1. Fuel cells, solar plants, and biomass are all examples of separate dc sources.
2. It is not feasible to switch between two converters in a back-to-back method.

3.1.3.2 Advantages

1. When obtaining the same number of voltage levels, a smaller number of components is required.
2. The use of additional capacitors and diodes is not required.
3. Scalable, modularized circuit architecture and packaging are both made possible by the fact that it has the same structure.

3.1.3.3 Disadvantages

1. Real power conversion requires separate DC sources.

See the graphic below for a representation of the model that was simulated using eight ideal switches. In order for each switch to function appropriately in a real-world setting, it is necessary for it to have its own specialised gate driver circuit. A direct current (DC) voltage of one hundred volts is used by the system, and the capacity of the load is established at ten ohms. Prior to the implementation of the Multicarrier PWM Techniques, simulations were carried out. These simulations included the comparison of a triangle wave with a constant value at particular time intervals, which ultimately resulted in a multistep output waveform that was not seen anywhere else. For the purpose of conducting an analysis of the harmonic spectrum based on the PWM techniques that were used, the FFT Window in MATLAB/Simulink was utilised.

3.2 Multiple-Level Inverters with Asymmetry

3.2.1 Binary-Based Multilevel Inverter

An illustration of the circuit layout of a cascaded H-bridge multilevel inverter that makes use of a binary DC input source may be seen in Figure 5. One of its defining characteristics is that it is able to take DC sources as input, despite the fact that it is similar to a standard cascaded H-bridge multilevel inverter. This particular inverter is capable of producing five separate output levels, which are -2Vdc, -Vdc, 0Vdc, and 2Vdc. It does this by using both Vdc and 2Vdc.

A basic output voltage with two levels is the responsibility of the lower inverter, which is responsible for creating it. After this, the upper inverter makes adjustments to the fundamental wave by either adding or deleting one level in order to produce stepped output waves. A consequence of this is that the final output voltage levels are established by

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adding together the voltages that are present at each terminal of the H-bridge. When the contributions from all terminals are added together, it is possible to represent the entire output in a mathematical manner. Through the use of this design, it is possible to efficiently assist the creation of numerous voltage levels while simultaneously preserving the integrity of the output waveform.

$$V_{out} = V_{HB1} + V_{HB2}$$

The predicted output voltage level is computed in the following manner in the circuit design that has been proposed: if there are *n* H-bridge modules linked in series, each of which has independent DC sources that follow a power of 2 arrangement, then the expected voltage level may be calculated accordingly. Using the features of the H-bridge modules, this design makes it possible to attain the appropriate voltage levels in an effective manner. This configuration also makes it possible to raise the output voltage in a methodical manner. Every new module makes a contribution to the total output, which results in an inverter design that is both adaptable and expandable, allowing it to accommodate a wide range of power needs.

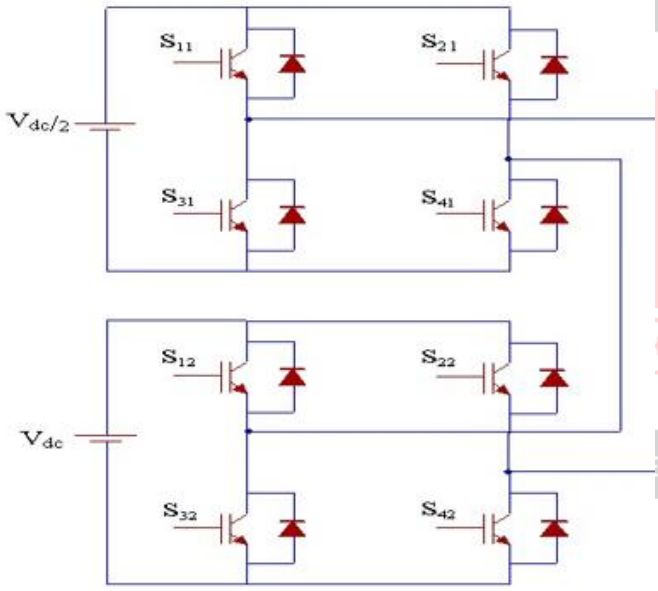

Fig. 5: H-bridge multilevel inverter utilizing a binary DC input source

3.2.2 Trinary multilevel inverter

The circuit layout of a cascaded H-bridge multilevel inverter that makes use of a trinary dc input source is seen in Figure 6. It seems to be a conventional cascaded H-bridge multilevel inverter, with the exception that it accepts dc sources as input. Because it makes use of Vdc and 3Vdc, it is able to generate five different output levels: -3Vdc, -Vdc, 0, Vdc, and 3Vdc. The lower inverter is responsible for producing a fundamental output voltage that consists of three levels. Subsequently, the higher inverter is responsible for adding or subtracting one level from the fundamental wave in order to produce stepped waves. In this case, the final output voltage levels are calculated by adding up the voltages at each terminal of the H-bridge, and the result is expressed as

$$V_{out} = V_{HB1} + V_{HB2}$$

In the circuit architecture that has been suggested, an anticipated output voltage level is provided as follows: if n number of H-bridge modules have independent DC sources in sequence of the power of 3, then the expected voltage level is:

$$V_n = 3^n,\ n = 1,2,3..$$

The FFT Window in MATLAB/Simulink was used in order to do an analysis of the harmonic spectrum, which was based on the PWM approaches.

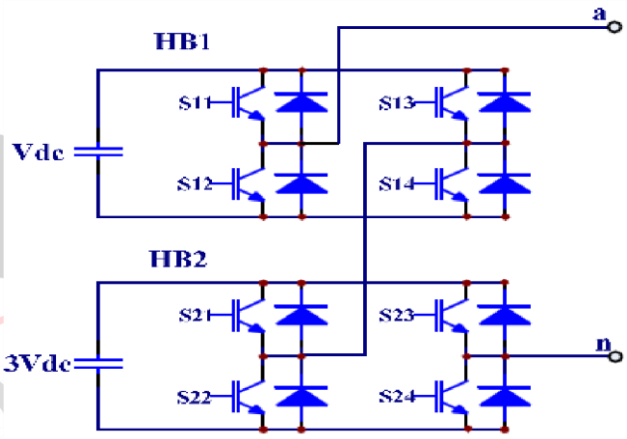

Fig. 6: H-bridge multilevel Inverter Utilizing a Trinary DC input source

3.2.3 Quadinary multilevel inverter

The circuit design of a cascaded H-bridge multilevel inverter that utilizes a quadinary DC input source is presented in Figure 7. While it resembles a standard cascaded H-bridge multilevel inverter, this configuration specifically accommodates DC sources as its input. By leveraging the input voltages of Vdc and 4Vdc, the inverter is capable of producing five distinct output levels: -4Vdc, -Vdc, 0, Vdc, and 4Vdc.

This architecture highlights the flexibility of the cascaded H-bridge design, allowing for the effective utilization of multiple DC input sources to achieve a broader range of output voltages. The integration of quadinary inputs not only enhances the inverter's capability to produce various voltage levels but also facilitates improved performance in applications requiring precise voltage regulation. As a result, this configuration is particularly advantageous in scenarios where space and component count are critical factors, enabling efficient operation without the need for excessive additional circuitry.

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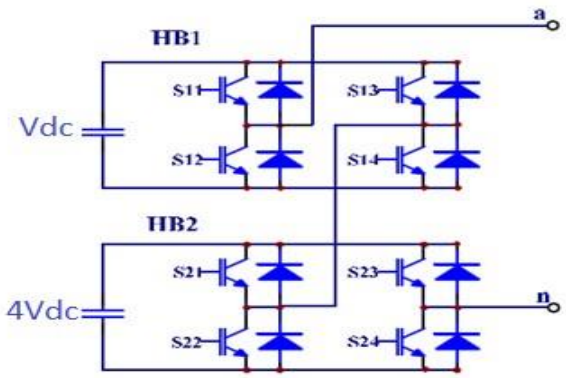

Fig. 7: H-bridge Multilevel Inverter Employing Quadinary DC input source.

The lower inverter generates a fundamental output voltage that includes four distinct levels. Following this, the upper inverter contributes by either adding or subtracting one level from the fundamental waveform, resulting in the formation of stepped voltage waves.

To determine the final output voltage levels, the voltages at each terminal of the H-bridge are summed together. This process allows for the precise calculation of the overall output voltage, reflecting the combined effect of the contributions from both the lower and upper inverters. The result is a comprehensive output that showcases the multi-level nature of the inverter, providing enhanced voltage granularity and improved performance in power conversion applications.

By utilizing this layered approach, the cascaded H-bridge inverter achieves greater flexibility in output voltage control, making it a valuable solution for various electrical systems that require high efficiency and adaptability.

$$V_{out} = V_{HB1} + V_{HB2}$$

Based on the proposed circuit architecture, the expected output voltage level can be determined as follows: if there are *n* H-bridge modules connected in series, each with independent DC sources and arranged in powers of 4, the anticipated voltage level is given by a specific formula. This structure allows for a systematic increase in output voltage as more H-bridge modules are added.

$$V_n = 4^n,\ n = 1,2,3..$$

Table 4. Comparison of components required for various topologies

S. No.	DCMLI (5-level)	FCMLI (5-level)	CMLI (5-level)	Binary MLI (7-level)	Trinary MLI (9-level)	Quadinary MLI (11-level)
Main switching devices	8	8	8	8	8	8
Clamping diodes	12	0	0	0	0	0
Balancing capacitors	0	12	0	0	0	0
DC bus capacitors	4	4	2	2	2	2
Main diodes	8	8	8	8	8	8

IV. CONCLUSIONS

This article presents a discussion and comparison of various multilevel inverter topologies. Compared to other inverter types, the cascaded multilevel inverter requires fewer components, as shown in Table 3. This results in a reduced number of semiconductor switches while achieving a higher stepped output. Fewer switches simplify the control of the entire circuit and minimize both size and installation space. If demand increases, additional H-bridges can be easily added to the cascaded inverter to accommodate the need.

Moreover, there are several innovative topologies for cascaded inverters that can help further decrease the number of switching devices required. Simulation results indicate that PWM methods using a comparison between triangular and constant values produced higher total harmonic distortion (THD) compared to multicarrier PWM techniques. The presence of significant lower-order harmonics made it inadvisable to use an amplitude modulation index below one with the filter design, although it did contribute to an overall reduction in THD. Ultimately, an ideal output is achieved with an amplitude modulation index equal to or less than one.

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